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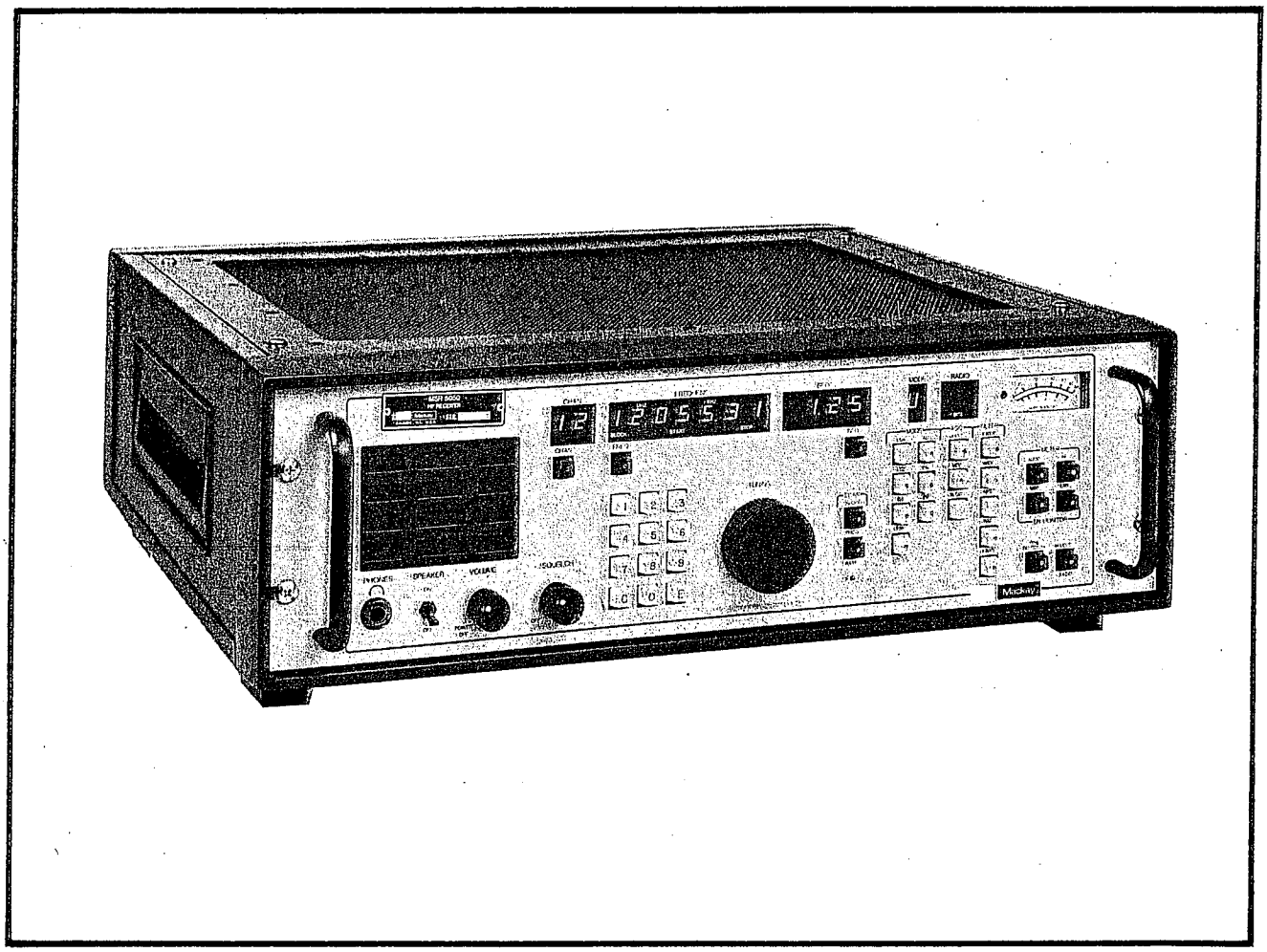

MSR 5050 Receiver

Issue 1

Publication No. 600249-823-001

NOTICE

MACKAY COMMUNICATIONS INC. reserves the right to make changes to the equipment without notice.

PROPRIETARY STATEMENT

SAFETY NOTICE

This equipment has dangerous RF voltages which can cause BURNS and INJURY. Do not touch the antenna connector, long wire antenna or metal portion of whip antennas when transmitting. When practicable, maintenance should be performed with the equipment de-energized. If power-on maintenance is required, use caution. Do not touch high voltage or RF components.

Mackay

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SECTION 1
INTRODUCTION

1.1 SCOPE

This instruction manual contains information necessary for the installation, operation and maintenance of the receiver.

1.2 DESCRIPTION

1.2.1 GENERAL

The MSR 5050 is a compact rugged, fully automatic, solid state receiver. It is designed as a continuous duty, HF/SSB receiver, covering the frequency range of 1 kHz to 30 MHz. The receiver is ruggedized and packaged to meet military specifications for vibration and shock environments.

The MSR 5050 is an HF communications receiver with capabilities comparable to the most advanced receivers in regard to ease of operation, reliability, cost-effectivity and maintainability.

Depending on the options specified, the MSR 5050 has the following capabilities:

1) Choice of direct frequency selection or sweep tuning - in one receiver!

2) Tuning in 10 Hz increments from 10 kHz to 30 MHz.

3) The MSR 5050 can automatically scan up to 99 easily programmed channels, either sequentially or in groups.

4) Frequency stability of 1 part in 10^6 as standard (1 part in 10^8 optional).

5) ISB

6) All usual reception modes, including LSB, USB, ISB, CW, RTTY, AM and NBFM (RTTY requires external modem).

7) Keypad selection of standard and optional bandwidths.

8) Provision for internal automatic preselector.

9) Computer control.

10) Remote control over telephone lines.

11) Synthesized precision BFO, with 10 Hz increments, for use when an offset, but very stable, BFO signal is required.

The receiver has been designed and constructed to facilitate quick and easy field service and/or repair. Featuring modular construction, the front panel, rear panel and power supply assemblies are removable with only a screw driver and the PC boards simply unplug from the mother board.

The receiver is composed of major subassemblies. A general description and function of these assemblies are provided in Sections 1.2.2 through 1.2.8.

1.2.2 CHASSIS/MOTHER BOARD

All subassemblies in the receiver are electrically or mechanically

connected to the chassis/mother board. The chassis houses all plug in PC boards and provides shielding. The mother board contains all interconnecting wiring in the receiver. All plug-in PC edge connectors. Keys on the connectors discourage plugging PC boards in the wrong slots.

1.2.3 FRONT PANEL ASSEMBLY

The front panel is a rugged aluminum assembly to which all controls and the speaker are mounted. The LED indicators and associated circuitry are mounted on the display and keypad boards which attach to the panel. The panel assembly can be removed from the receiver, by removing four nuts, three screws and four cable connectors.

1.2.4 LOGIC BOARD

The logic board contains the microprocessor, memory and receiver control logic. The receiver channel memory is a CMOS type which is kept alive by a lithium battery with a 10 year typical life. Signals from the logic board provide frequency information to the synthesizer; and band, filter, AGC, and mode information to the receiver modules.

1.2.5 RECEIVER SIGNAL PATH

The receiver signal path consists of six PC boards: (1) speaker amplifier, (2) audio/squelch, (3) IF filter, (4) mixer, (5) high pass filter, and (6) low pass filter.

The receiver signal path processes the received signal from the antenna to the speaker, using inputs from the synthesizer.

A double conversion scheme is used, with the first intermediate frequency (IF) at 59.53 MHz and the second IF at 5.00 MHz. Two sets of crystal filters (one set at each IF) determine the radio bandwidth.

1.2.6 SYNTHESIZER

The synthesizer consists of four PC boards: (1) major loop, (2) translator loop, (3) minor loop and (4) reference board. The synthesizer is a three loop design which provides the receiver with the first local oscillator (LO) from the major loop board, the second LO from the translator loop board and the third LO from the reference board to the receiver. All frequencies are derived from a temperature compensated crystal oscillator (TCXO) on the reference board. If a fault causes any of the loops to lose lock, the loss-of-lock LED will light on the appropriate board(s), reception will be inhibited, and the front panel BITE display will indicate code E1.

1.2.7. REAR PANEL ASSEMBLY

The rear panel assembly is an aluminum assembly which contains the power supply assembly and various external interface connectors. It attaches to the receiver chassis with nine screws and is easily removable as a unit.

The power supply assembly is a linear type operating from 115 or 230 VAC. It consists of a PC board assembly mounted to a heatsink containing pass transistors which supply the +5, +9, and +13 VDC for the receiver. The assembly is removable from the rear panel by four screws. Electrical disconnect is via two molex connectors.

1.3 TECHNICAL SPECIFICATIONS

All specifications at 115 VAC, 60 Hz operation at 25°C unless otherwise specified.

Frequency Range	10 kHz to 30 MHz in 10 Hz increments.
Tuning Controls	Keypad entry or continuous tune by variable rate TUNE knob.
Frequency Stability	± 1 PPM (standard) ± .01 PPM (option)
BFO Tuning Range	± 9.99 kHz (10 Hz steps)
BFO Tuning Control	Keypad entry or continuous tune by variable rate TUNE knob.
Channel Operation	
Channel Storage	Up to 99 channels programmable for frequency, BFO, AGC speed, Mode and IF bandwidth by keypad.
Channel Scan	Automatic scan of channels in memory in 6 programmable blocks.
Sensitivity	SSB: -113 dBm for 10 dB (S+N)/N AM (6 kHz bandwidth): -97 dBm for 10 dB (S+N)/N CW 2.7 kHz bandwidth): -113 dBm for 10 dB (S+N)/N FM (with option): -97 dBm for 10 dB (S+N)/N (Sensitivity degraded 6 dB below 2 MHz in addition to 6 dB per octave below 0.5 MHz).
Operating Modes	Standard: AME (A3H), CW (A1), LSB, USB (A3J upper and lower), and FSK (F1 with optional external modem) Optional: ISB (A3B) and NBFM (F3)

Selectivity (Fc = 5.000 MHz)

BANDWIDTH	MODE	6dB BANDWIDTH	60 dB BANDWIDTH
*VWide	AM, CW, FSK, FM	12 kHz Min (3dB)	40 kHz Max
Wide	AM, CW, FSK	5 kHz Min	18 kHz Max
Med	AM, CW, FSK	2.7 kHz Min	6 kHz
*Narrow	AM, CW, FSK	1 kHz Min	6 kHz Max
*VNar	AM, CW, FSK	400 Hz Max	4 kHz Max
Med	USB	≤300 & ≥3000Hz	≥-1.5 & ≤4.5 kHz
Med	LSB	≥-300 & ≤-3000 Hz	≤1.5 & ≥-4.5 kHz
*Med	ISB	Same as USB & LSB	Same as USB & LSB

*Optional Equipment
NOTE: Optional FM board includes separate VWide filter which is used only when FM mode is required.

IF and Image Rejection	80 dB minimum
External Spurious Rejection	70 dB minimum
Internal Spurious Rejection	99.5% below 0.2 μV
Intermodulation Distortion (In Band)	For two equal 0.1 volt input signals that produce tones of 1100 and 1700 kHz, the IM products shall be at least 30 dB below the audio tones.
Intermodulation Distortion (Out-of-Band)	Two 3 mV signal at +30 and +60 kHz removed from the receiver frequency shall produce less audio output than a 1 μV desired signal.
Crossmodulation	With a desired signal of 100 μV unmodulated, the level of an interfering 30% modulated signal ± 100 kHz from the desired signal shall be at least -18 dBm to cause an audio output 20 dB below the reference.
Blocking	With a desired signal of 50 μV, the level of an undesired signal removed ± 30 kHz shall be at least -14 dBm to reduce the audio output by 3 dB.
Oscillator Reradiation	Signals at the antenna connector due to internal oscillators (59.54 -89.53 MHz first L.O.; 54.53 MHz second L.O.; 5.0 MHz third L.O.) shall be less than -73 dBM (2 to 30 MHz) and less than -55 dBm (<2mHz).
Unwanted Sideband Rejection	The response of a signal 1 kHz below/above tuned receiver frequency shall be down 50 dB in USB/LSB mode with respect to the response in LSB/USB mode.
Audio Output	Not less than 4 watts at 10% maximum distortion into 3 ohms load.
Speaker	Not less than 10 mW at 5% maximum distortion on into 600 ohms.
Phone	Internally adjustable (Audio Squelch Board) from less than -10 to not less than +10 dBm at not more than 5% distortion into 600 ohms.
Standard and Optional ISB 600 ohm line	Not less than 34 dB at 100 μV, SSB mode.
Ultimate (S+N)/N	

Mute	Speaker and phone audio reduced 50 dB by external TTL signal (rear panel).
Squelch	Mutes speaker and phone audio by front panel control with threshold adjustment from noise to 30 μV.
Diversity	In USB both IF's controlled by the IF AGC with the largest signal for frequency diversity; inputs and outputs of AGC from each IF available for space diversity.
AGC	
Range	-97 to +13 dBm with less than 10 dB change in audio output (measured in SSB)
Attack-Time	Less than 10 milliseconds (AGC FAST)
Decay Time	(For 60 dB change in signal) AGC FAST - not greater than 50 mSec.; 30 mSec. typical. AGC Medium - 150 mSec. Min., 350 mSec. Max., 200 milliseconds nominal.
Antenna Input Protection	Protection up to 22 volts at 50 ohms.
Dimensions	Height 5.25 inches; width 19 inches; depth 17 5/8 inches (Exclusive of controls, connectors and handles).
Weight	30 pounds Max.
Power	115/230 VAC (+ 10% to specification, + 15% operational; 47 to 400 Hz, 75 watts Max.
Temperature	-10°C to +50°C - (115 VAC or 230 VAC)
Humidity	95% at +50°C for 24 hours
Shock	MIL-STD-810C, Method 516.2, Procedure V
Vibration	MIL-STD-810C, Curve AW, Method 514.2, Procedure X, Modified to 1.5 g from 5.5 to 50 Hz.

1.4 EQUIPMENT SUPPLIED

1.4.1 RECEIVER -Part Number 690024-000-XXX

1.4.2 KIT, ACCESSORY - Part Number 690024-017-001 consisting of:

a) Connector, Accessory, Part Number 600292-606-005

b) Fuses, 1 Amp, Slo-Blo (1) - Part Number 600006-396-019

c) Fuses, 0.5 Amp, (1) - Part Number 600006-396-014

d) Connector, RF, PL-259 - Part Number 600244-606-001

e) Card Puller - Part Number 600268-618-001

f) Cable, Power - Part Number 600078-102-001

1.43 Manual, Technical, Part Number 600249-823-001

1.5 OPTIONAL EQUIPMENT — NOT SUPPLIED

I.F. Filter Option:

Filter Option. Provides the following bandwidths. USB/LSB 2.7 kHz, CW/AM (v. wide) 12 kHz, CW/AM (wide) 6 kHz, CW/AM (narrow) 1 kHz, CW/AM (v. narrow) 400 Hz, CW/AM (medium) 2.7 kHz, Part Number 600083-700-001.

NOTE

BFO Option must be specified for reception of CW, RTTY or Data using 1 kHz or 400 Hz filters.

BFO Option:

Synthesized BFO tunable from 0 to + 9.99 kHz in 10 Hz steps. Recommended when Filter Option is specified. Part Number 600107-700-001.

Independent Sideband Options:

ISB Option "A". Specify this when the filter option is not installed. Reconfigures radio for ISB operation and provides additional audio channel for ISB. Same bandwidths as Filter Option "A". Part Number 600086-700-001.

ISB Option as above, except for use with Filter Option "B". (Part Number 600083-700-001) only. Same bandwidths as standard radio. Part Number 600086-700-002.

FM Option:

Provides capability for FM reception bandwidth (3dB) = 12 kHz min. Part Number 600085-700-001.

High Stability Option:

Oven controlled crystal oscillator provides stability of 1 part in 10^8. Part Number 600090-700-001.

Remote Control/Computer Control Options:

NOTE

Only one of the following options may be fitted in one receiver.

Current Loop/RS232/RS423 MIL 188 option: Internal modem gives choice of control; either by Current Loop or by RS232 interface at data rates from 50 to 9600 baud. Used for control of MSR 5050 by computer or by MSR 6406 Remote Control Unit. Part Number 600087-700-001.

FSK Remote Control Option: Internal modem allows MSR 5050 to be controlled at 300 baud rate by MSR 6406 Remote Control Unit over standard 2-wire telephone circuit. Additional circuit(s) required for transmission of received audio signals. (For 1200 baud data rate, specify instead external type 212 modem and 600087-700-001 RS232 option). Part Number 600087-700-002.

Voice-Plus Remote Control Option: Internal modem allows interconnection of MSR 5050 and MSR 6406 Remote Control Unit by a single 2-wire telephone circuit. (A second 2-wire circuit is required for ISB audio, if applicable). Data rate is 150-300 baud. Part Number 600164-700-001.

IEEE 488 Option: Internal modem provides capability for computer control of MSR 5050 using IEEE 488 interface. Part Number 600082-700-002.

Miscellaneous Options:

Desk Top Cabinet (Black): Allows the MSR 5050 to be installed as a free-standing desk-top system. Overall dimensions of the MSR 5050 installed in cabinet; W - 19 3/4" X D - 19 1/4" X H - 6 3/4". Part Number 600077-700-001.

Rackmount Kit: Rack slides and hardware allow MSR 5050 to be installed in standard 19" rack. Part Number 600078-700-001.

Spare PCB Kit: Contains one each of all plug-in PCB assemblies. Allows on-site servicing by substitution of modules. Part Number 600079-700-001.

Comprehensive Spares Kit (CSK): Intended for on-site or depot repair of MSR 5050 with minimum downtime. Contains PCB assemblies, other assemblies and some piece parts. One CSK should support up to five MSR 5050 receivers for 2 - 4 years. Part Number 600165-700-001.

Depot Spares Kit (DSK): Includes individual components required to repair defective MSR 5050 assemblies, and other parts not included in CSK. DSK is intended for use at Depot level by trained technicians and, with the CSK Kit, should support up to five receivers for 2-4 years. Part Number 600080-700-001.

Extender Board Kit: Maintenance aid provides means to extend any plug-in PCB in MSR 5050. (Particularly applicable for Depot level maintenance in conjunction with DSK kits). Part Number 600081-700-001.

MSR 6406 Full Function Remote Control Unit: Provides full function serial remote control for frequency mode, channel select, meter reading and address for receivers set in multiple control configuration. Part Number 699026-000-XXX.

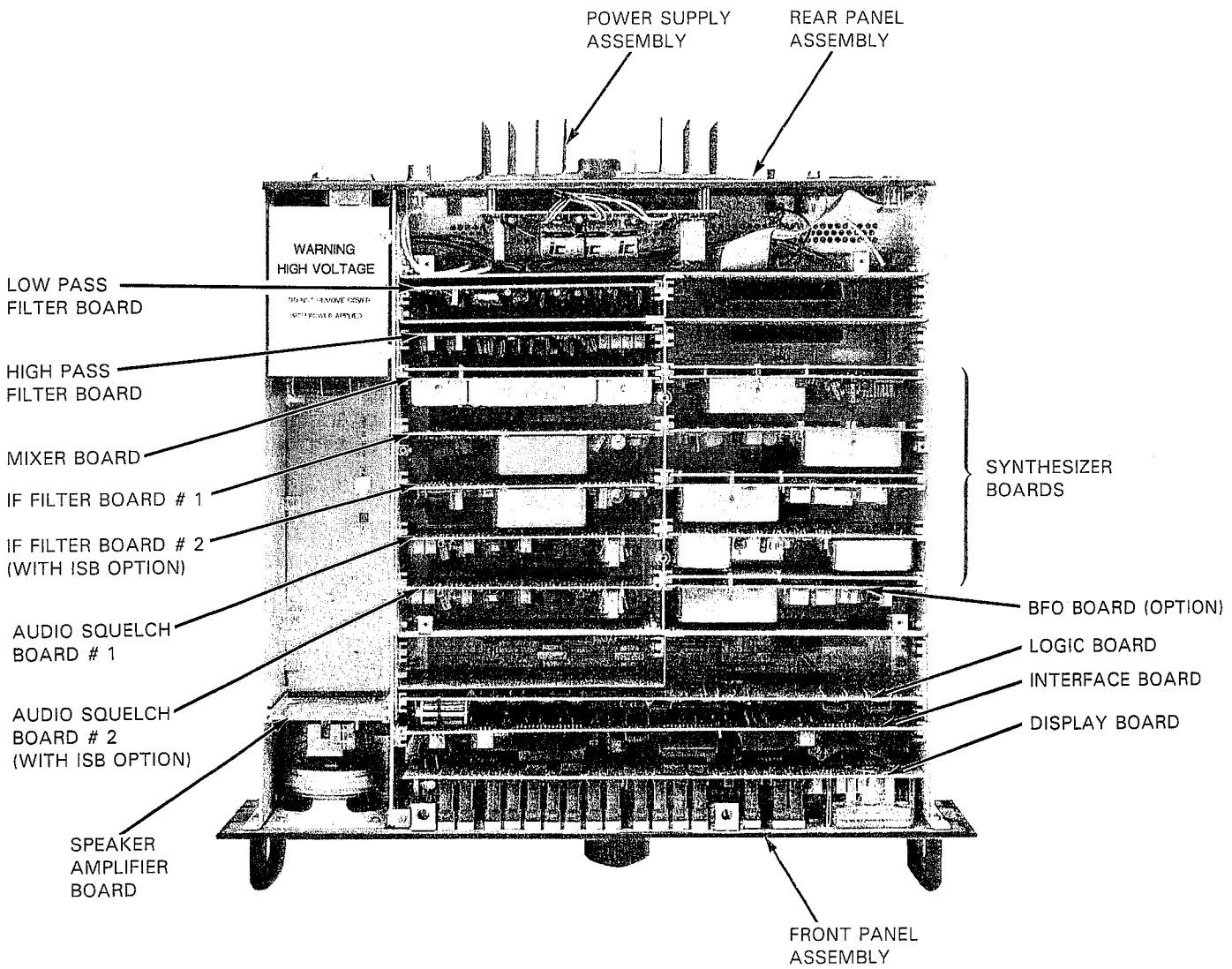


FIGURE 1.1 MAJOR SUBASSEMBLY LOCATIONS

SECTION 2
INSTALLATION

2.1 GENERAL

This section describes the installation procedure for the receiver. Installation of the receiver is quick and simple as the unit is completely wired, calibrated and tested before shipment from the factory. Included within this section are procedures for unpacking, inspection and, if necessary, reshipping.

2.2 UNPACKING AND INSPECTION

Unpack the receiver and make certain that all equipment outlined in Section 1.4 is present. Retain the carton and packing materials until the contents have been inspected. If there is evidence of damage, do not attempt to use the equipment. Contact the shipper and file a shipment damage claim.

2.3 RESHIPPING

If return of the receiver should become necessary, a Returned Material (RM) number must first be obtained. This number must be clearly marked on the outside of the shipping carton.

2.4 INSTALLATION

Thoroughly plan the receiver/antenna locations and carefully follow the installation considerations given below. Satisfactory system performance depends upon the care and attention taken prior to and during installation.

The protective connector covers installed on the receiver for shipping should remain over unused connectors.

2.4.1 REAR PANEL

All external connections are made to the receiver's rear panel. Mounted on the rear panel are the following connectors.

WARNING

Before connecting power, check voltage selector card and fuse located under power cord.

A) AC POWER - Standard AC Power connector. To change AC input voltage, the line cord in unplugged from the assembly. Then the plastic cover is slid down exposing the fuse/selector card chamber. The operating voltage is indicated by the exposed numbers on the card. By top-to-bottom, the operating voltage may be changed from 115 volts (marked 120), TO 230 volts (marked 240), to 100 volts (marked 100), to 220 volts (marked 220). Operation VAC $\pm$ 15% is possible by selecting the 100V or 220 VAC position. The appropriate fuse must be installed when the operating voltage is changed. (See Fuses in Section 3.3.2).

B) ANTENNA (J46) - An SO-239 type connector.

C) GND - A 1/4 -20 chassis ground stud.

D) FUSE - 1A for 115V or 0.5A for 230V.

E) SIGNAL IN/OUT (J42) - A 25-pin miniature "D" connector containing the audio line outputs, two-wire remote control lines, and current loop lines, and spare lines for future use. See Table 2-1.

F) RS-232 (OPTIONAL) - A 25-pin miniature "D" connector containing signals for the optional RS-232 interface. The connector will not be installed and the hole will be covered if the option is not installed.

G) IEEE 488 (OPTIONAL) - This is the 24-pin micro ribbon connector specified for 488. The connector will not be installed and the hole will be covered if the option is not installed.

H) REF IN/OUT - A BNC for the 5 MHz reference. Rear panel switch determines whether this is an input or output.

I) IF MONITOR - A BNC which provides a 5 MHz IF output signal at 50 ohms.

2.4.2 INSTALLATION CONSIDERATIONS

2.4.2.1 Antenna Site Location

For optimum characteristics and safety, the antenna should be mounted high enough to clear any surrounding obstructions. The antenna should also be located as far as possible from nearby objects such as power lines, buildings, etc.

2.4.2.2 Adequate Ground

Provide the best possible RF ground for the receiver and the antenna. Use a flat copper strap, 25 mm wide or number 6 gauge or larger wire and connect it to the ground terminal at the rear of the receiver and on the antenna. Leads to the ground system should be as short as possible.

2.4.3 BASE STATION INSTALLATION

The receiver can be installed in its own (optional) cabinet for table-top mounting or can be installed in communications console.

It is important to provide adequate ventilation for the heat-sink. Clearances on the order of 25 mm on the sides and 50 mm at the top and rear should be provided.

2.4.3.1 RACK MOUNT INSTALLATION

The receiver may be conveniently mounted in a standard 19 inch rack, by using the rack mount kit (P/N 600078-700-001). This kit includes a pair of rack slides, and associated hardware. The receiver in the rack mounted configuration requires a standard panel space of 13.21 cm (5.2 inches).

The front panel is not designed to support the receiver when the unit is installed in an equipment rack.

CAUTION

Do not support the receiver by the chassis bottom in such a way that the air flow will be restricted.

If installation assistance is required, consult the ITT Mackay Service Department.

2.4.4 MARINE INSTALLATIONS

The receiver is not weather, splash and corrosion resistant, and should not be installed where it is exposed to salt spray. It should be installed in a well ventilated area away from heat sources such as heating vents, etc. The location should

Table 2-1

SIGNAL IN/OUT CONNECTOR (J42) PIN ASSIGNMENTS

PIN	LINE NAME	DESCRIPTION
1	Current Loop RX1	Control Lines for Optional Current Loop Remote Control
2	Current Loop TX2	
3	Current Loop TX1	
4	RF Gain A	External control lines: 0 to +9 volts varies gain from maximum to minimum (>100 dB) on Standard (A) output and optional ISB (B) output
5	RF Gain B	
6	+5 volts DC	+5 volts from internal supply
7	DC Ground	
8	DC Ground	
9	DC Ground	
10	Sidetone	External Input (1kHz) 0 dbm, 600 ohms to produce speaker output
11	AGC B	AGC voltage output (0 to 6 VDC) from optional ISB (B) IF channel
12	Spare	
13	Spare	
14	Current Loop RX2	Control Line for Optional Current Loop Remote Control
15	FSK 600 A	Control Lines for Optional FSK Remote
16	FSK 600 B	
17	Speaker Return	Output for External Speaker 3 ohms/4W
18	Speaker	
19	Scan Detector	Output to indicate signal presence during channel scan (TTL low)
20	Mute	External Signal (TTL low) to mute speaker audio
21	ISB 600 B	600 ohm audio line output from optional ISB channel
22	ISB 600 A	
23	STD 600 B	600 ohm audio line output from standard receiver
24	STD 600 A	
25	AGC A	AGC voltage output (0 to +6 VDC) from standard receiver IF channel

be as close as possible to the power source and grounding point.

IT IS RECOMMENDED THAT THE RECEIVER BE SECURELY GROUNDED, as poor grounding can degrade performance. With a metal hull, the receiver can be grounded directly to the vessel's structure. With a wood or fiberglass hull, a ground/counterpoise system must be constructed. The counterpoise should have as much surface area as possible. About 9.5 square meters (100 square feet) should be provided for 2 MHz operation. A reasonably good ground can be achieved by bonding together large metal objects. Bonded to this ground should be two or three wide copper straps running as far as possible fore and aft, together with three or four cross members (ground plates may be effective on lower frequencies but are subject to fouling. Therefore, they are not recommended). Figure 2.1 shows a typical ground/counterpoise system.

2.5 ANTENNAS AND GROUND SYSTEMS

The receiver is designed to operate from a 50 ohm resistive antenna system. VSWR should be low to ensure optimum performance.

Some general antenna system guidelines are:

a) Mount the antenna as high as possible.

b) Where possible, use antennas over 1/8 wavelength long at the lowest operating frequency.

c) Short antennas are most sensitive to ground loss. When a short antenna is used, the best possible ground system should be obtained.

d) On ships with non-metallic hulls, make the ground/counterpoise system cover as large an area as possible. Make maximum use of large metal objects, copper screen, the propellor shaft and properly bonded copper straps.

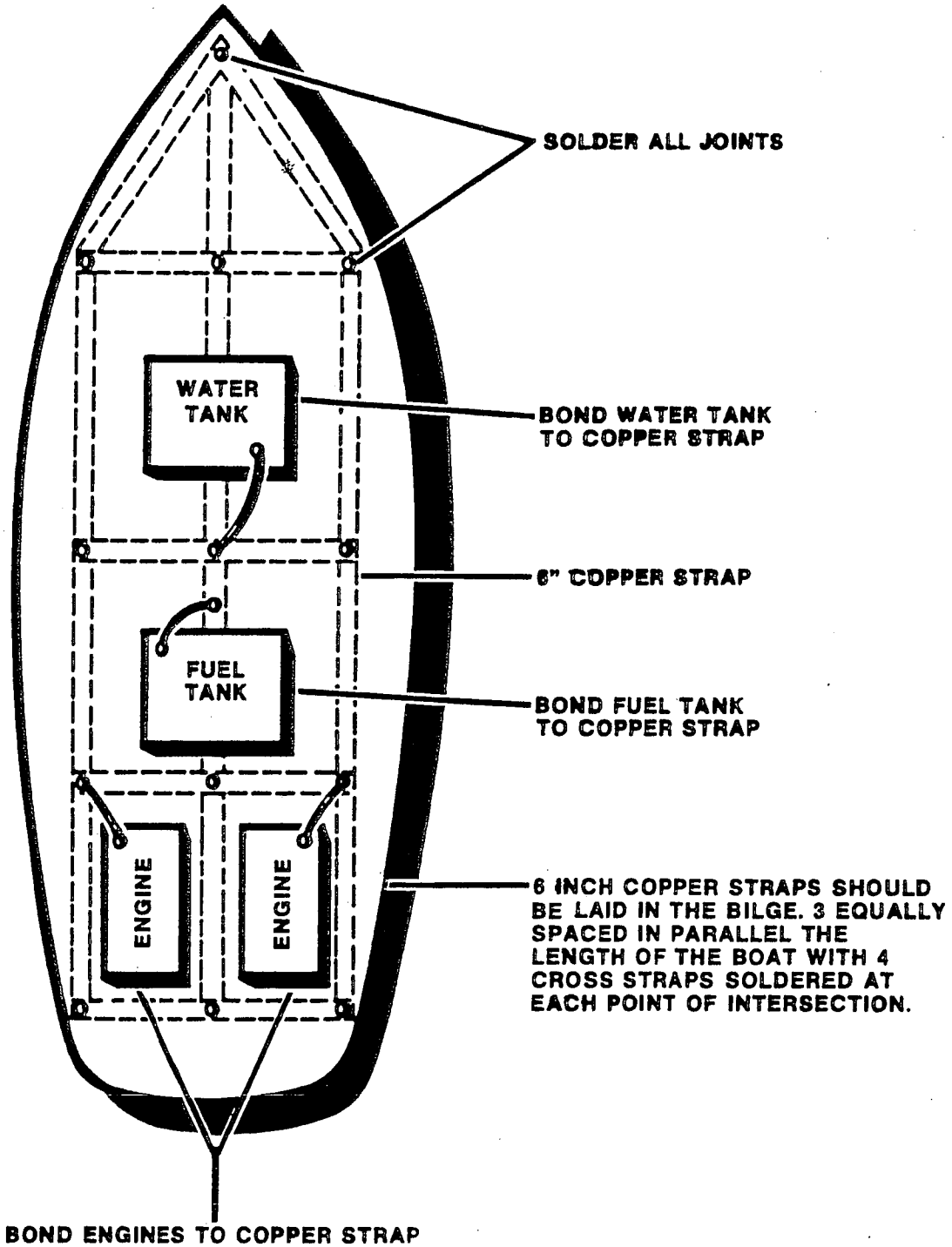


Figure 2.1 Typical Ground/Counterpoise Installation

SECTION 3
OPERATION

3.1 GENERAL

This section describes the control and connector functions and gives complete operating instructions for the receiver.

3.2 FRONT PANEL CONTROLS AND CONNECTORS

(Refer to Figure 3.1 for control locations).

NOTE

All front panel function switches contain LEDs (Light Emitting Diodes) to indicate when a particular function is active.

3.2.1 HEADPHONE JACK

The headphone jack accepts a standard 1/4" two circuit plug from the headphones. Using the headphone jack does not cut off the speaker. Headphone impedance of 600 ohms or more is recommended.

3.2.2 SPEAKER SWITCH

Turns the internal speaker on and off.

3.2.3 VOLUME/POWER

Controls the received signal level at the speaker and PHONES jack. Click-off CCW position turns off receiver primary power. VOLUME setting does not affect 600 ohm receive audio output.

3.2.4 SQUELCH

Rotary action sets the squelch threshold. The squelch is defeated in fully CCW position (maximum threshold is fully CW).

3.2.5 CHANNEL

Pressing this button clears the CHAN/FREQ display and permits selection of an existing, programmed channel, or the entry of new channel and frequency information; pressing FREQ button alone clears the channel display to 00, or "scratch pad" status to permit independent frequency selection; when channel and frequency are entered, the display flashes until the "C" or "E": key is pressed.

3.2.6 FREQUENCY

Pressing this button clears the FREQUENCY display and causes the CHAN display to indicate 00, or a "scratch pad" condition for independent entry of frequency; after selecting frequency, pressing the "E" key will enter it, while pressing "C" (Clear) will restore the previously selected channel and frequency.

3.2.7 TUNING KNOB

The tuning control knob fine-tunes the receiver in 10 Hz steps to center the received signal in the IF passband. Maximum tuning rate is approximately 10 kHz per second. Meter or speaker indications may be used as an aid in tuning. Large frequency changes should be implemented by the keypad.

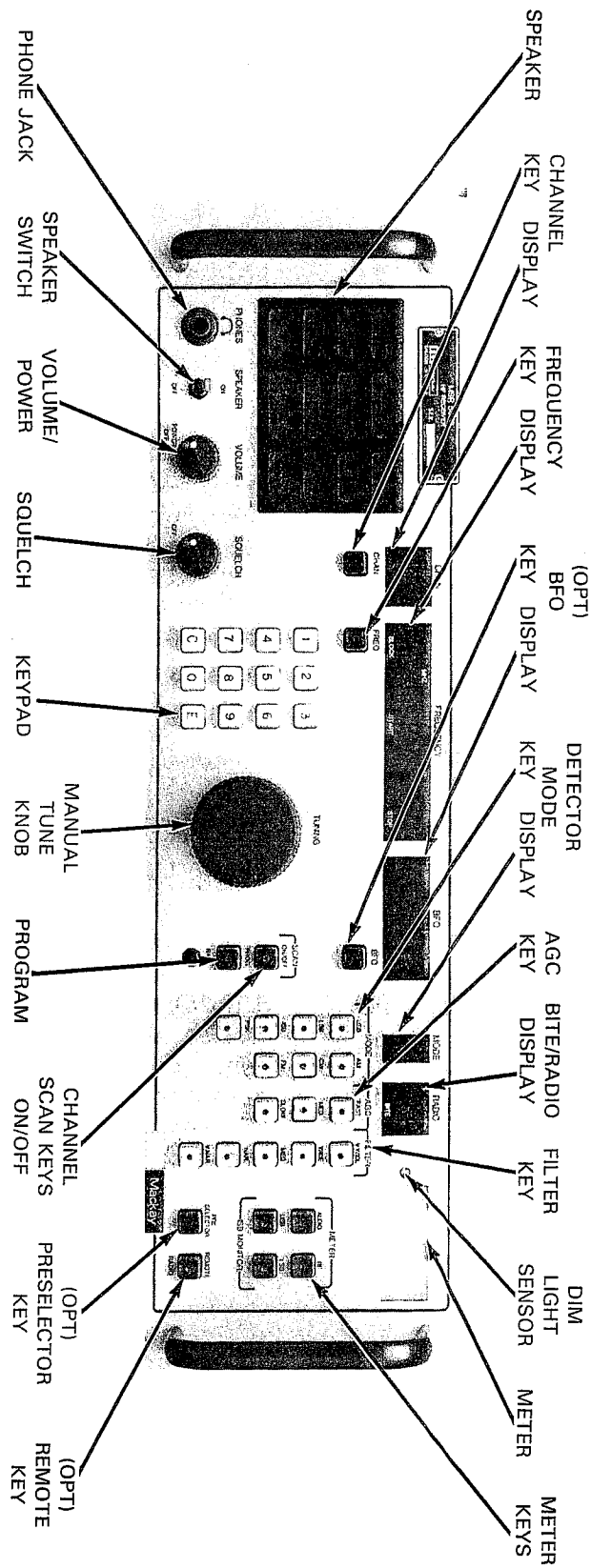


Figure 3.1 Front Panel Controls

When the BFO option is installed, the TUNE knob also fine tunes the BFO in 10 Hz steps from .+9.99 to -9.99 kHz. The knob is changed to BFO control by pressing the BFO switch. The switch key lights to indicate BFO control. Pressing "E" (enter) or "C" (clear) returns the knob to frequency control. To quickly remove BFO offset and return to 000 (normal SSB setting), press "BFO" and "C".

3.2.8 BFO (OPTIONAL)

Press BFO switch key once for positive offset number keypad entry or variable knob tuning. Press switch twice for negative numeric entry. Tuning range is 0 to ± 9.99 kHz in 10 Hz steps. To quickly remove BFO offset and return to 000 (normal SSB setting), press "BFO" and "C".

BFO is used to alter the demodulated tone from the product detector (CW, SSB, FSK). It is commonly used to produce audio tone (i.e. 1 kHz) from a CW signal received in the center of the receiver IF passband in a narrow filter.

3.2.9 SCAN

Preprogrammed channels may be automatically scanned in up to six blocks containing a maximum of 99 sequential channels. The start and stop frequency, of each block to be scanned, may be programmed in the SCAN PROG mode. The scan rate is adjustable by means of a screw adjustment located under the PROG switch.

3.2.10 MODE SWITCH

Pressing any of these switches will set the receiver operating mode during programming. On a currently operating channel, pressing any of these switches will actively change the receive mode without changing the originally stored program information.

3.2.11 AGC FAST/MED/SLOW

The AGC FAST/MED/SLOW keys control the AGC delay time, FAST equals 30 milliseconds nominal, MED equals 200 milliseconds nominal and slow equals 1.5 seconds nominal. Although the AGC rate is automatically determined when the mode is selected, the AGC rate may also be selected from the front panel switches if desired.

3.2.12 FILTERS

The filter switches select bandwidths of very narrow (VNAR), narrow (NAR), medium (MED), WIDE and very wide (VWIDE). Although the filter is automatically determined when the mode is selected, the filter may also be selected, in CW, AM and FSK modes from the front panel switches. In USB, LSB, and ISB modes all filter selections are locked out except MED. In FM all filter selections are locked out except VWIDE. The MED and WIDE filters are standard. All others are optional.

3.2.13 PRESELECTOR (OPTIONAL)

Provisions have been made to incorporate a preselector which will be electrically inserted in the RF signal path to add a narrow bandpass response to enhance operation in high signal level environments. The preselector, normally bypassed, will be engaged by a front panel switch. Tuning will be automatic as a result of a change in receiver frequency.

3.2.14 REMOTE/RADIO

Selecting remote disables the keyboard (except meter and speaker functions) and enables remote control operation. Selecting this function on the remote control

unit clears the "Radio" display, and allows entry of a number (up to 99) representing a receiver which is to be controlled by the remote unit. This switch has a "push-push" action on the MSR 6406 Remote Control Unit.

3.2.15 METER

The meter displays either RF or 600 ohm audio signal levels as selected by the RF or audio switches . With the ISB option the meter will respond to either the LSB or USB IF channel, in the ISB mode, as selected by their respective switches. Simultaneously the front panel speaker and phones jack, will also respond to the selected sideband.

3.2.16 DIMMER

A photosensor is incorporated in the front panel to sense ambient light and automatically adjust the brightness of the displays and status LEDs.

3.2.17 BITE INDICATOR

The front panel Built In Test Equipment (BITE) indicator will indicate a fault in one of the major internal subassemblies.

3.3 REAR PANEL CONTROLS AND CONNECTORS

Refer to Figure 3.2 for locations.

3.3.1 POWER CONNECTOR

Accepts standard AC input of 115 V or 230 VAC ±15% 47 to 63 Hz. Operating voltage is selected by a printed circuit card plugged into the connector assembly.

3.3.2 FUSES

Fuses are slo-blo type. 1A 115 VAC or 0.5A 230 VAC.

3.3.3 EXTERNAL REFERENCE INPUT (J41)

A BNC jack accepts an external reference frequency input depending on the adjacent switch position.

3.3.4 EXT/INT REFERENCE SWITCH

EXT/INT reference switch selects an externally applied reference signal, or the internal reference. The switch is located on the rear panel by J41.

3.3.5 IF MONITOR (J45)

A BNC jack outputs a 5 MHz IF signal for external monitor.

3.3.6 ANTENNA CONNECTOR (J46)

Connects RF input to the receiver. Mates with standard PL-259 connector.

3.3.7 GROUND STUD

Used for making good RF ground to receiver.

3.3.8 SIGNAL IN/OUT (J42)

Connects 600 ohms balanced audio lines and miscellaneous control and monitor lines. (See Table 2-1).

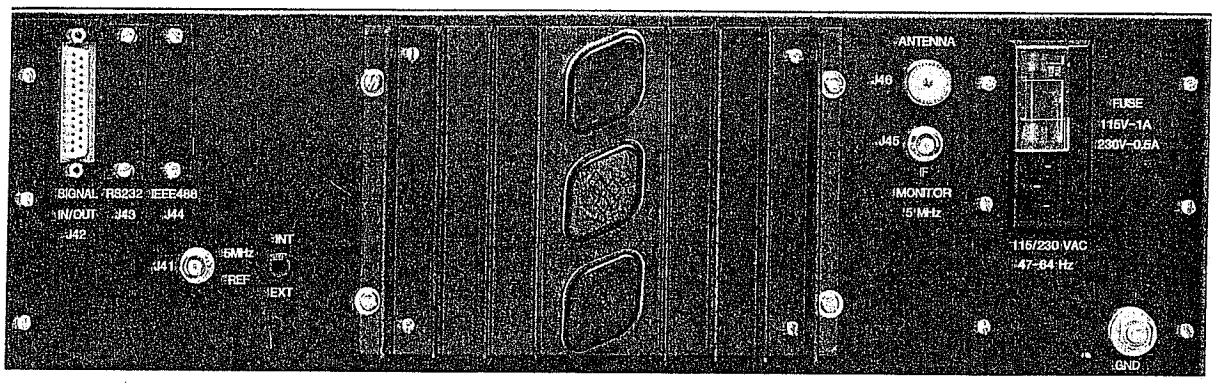


Figure 3.2 Rear Panel Controls and Connectors

3.3.9 REAR PANEL CUTOUTS (J43, J44)

For optional RS232 and IEEE 488 interfacing.

3.4 OPERATOR INTERNAL CONTROLS

Refer to Figure 3.3 for locations.

3.4.1 LINE VOLTAGE

Selects line voltage input of 115 VAC or 230 VAC.

3.4.2 600 OHM RECEIVE OUTPUT LEVEL

This control (R54) adjusts the level of 600 ohm receiver audio that can be supplied from the receiver to remote sources or optional equipment. Nominal output is 0 dBm, adjustable to +10 dBm.

An identical control is available for ISB when the ISB option is installed.

3.4.3 SCAN DELAY (R60)

This control sets the time (.5 to 5 seconds) the receiver stops on a channel occupied by a signal above the threshold. Threshold may be varied by the front panel squelch control.

3.5 OPERATION

The MSR 5050 Receiver is designed to operate in three different operating modes: manual, channel, and frequency. The following are step by step instructions in the operation of the receiver in each of the three operating modes.

3.5.1 MANUAL MODE OF OPERATION

The manual mode is used primarily to search for signals or to modify receiver characteristics to optimize reception. Controls may be operated freely without fear of affecting stored data. The only way to modify stored channel data is to press CHAN, XX and then E (enter). Proceed typically by the following steps:

a) Connect a 50 ohm antenna to the ANTENNA connector.

b) Connect the headphones or switch speaker ON. Turn power switch to ON and advance VOLUME control aproximately 1/3 rotation.

c) Turn SQUELCH control fully CCW.

d) Verify that the REMOTE/RADIO function is off.

NOTE

If the REMOTE/RADIO switch is pressed, the front panel keypad and control functions will be "locked out", and in the remote control operating mode.

e) Press the desired METER switch to display RF or audio signal level.

f) Tune the receiver to the desired frequency by turning the TUNE knob, either clockwise or counterclockwise, until the desired frequency is displayed on the front panel of the receiver.

g) Select the desired operating mode, AGC decay rate, and IF Filter by pushing their respective switches. The switch LED indicators will light as each switch is made.

h) The unit should now receive. The volume may be adjusted to a comfortable level.

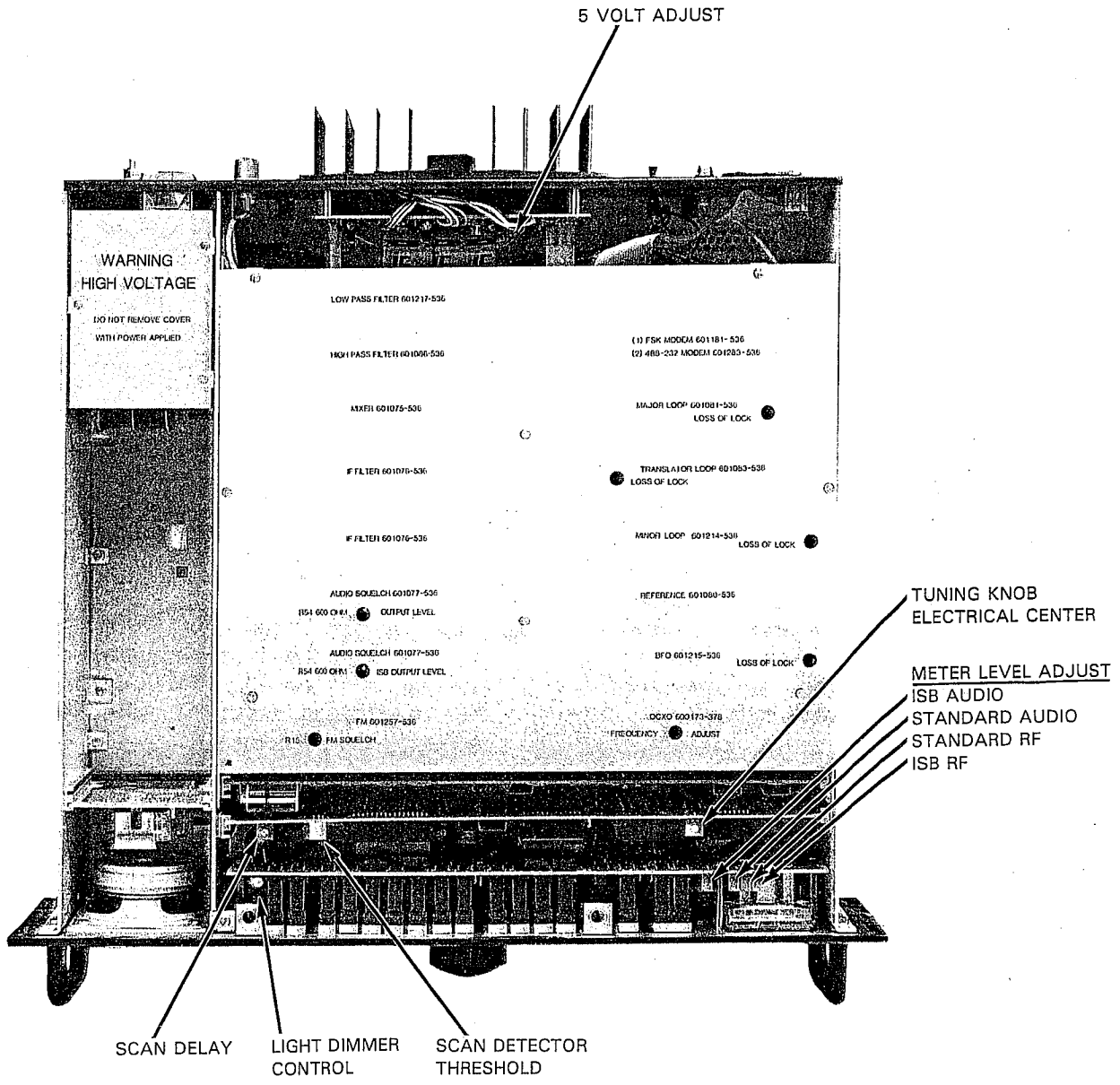


Figure 3.3 Internal Controls Location

i) The SQUELCH control may now be turned slowly clockwise to a position where background noise is squelched during periods when no signal is present. This is the point of minimum squelch threshold, and further clockwise adjustment beyond this point will require a stronger received signal to cause an audio output.

j) If required, all frequency, BFO, mode, AGC and IF filter information may be stored in memory for later recall. To program memory proceed as follows:

1) Press "FREQ". The FREQUENCY display will go blank and the "CHAN" display will read 00.

2) Press "CHAN". The CHAN display will go blank and the previously displayed frequency will re-appear.

3) Select desired channel number (single digit number is preceeded by 0). Press "E" to enter displayed information into the receivers memory.

3.5.2 CHANNEL PROGRAM MODE OF OPERATION

The channel program mode of operation is used primarily for frequencies which will require frequent recall or surveillance. The MSR 5050 Receiver has the capability to store in memory up to 99 frequencies with associated BFO, mode, AGC, and filter in 99 different channels. The following are step-by-step instructions for channelized operation:

NOTE

Before the memory is programmed for the first time, or if the battery has been removed from the logic board, the display may contain strange characters or blank digits on some channels. This is normal. Proper digits will return as the desired frequency is programmed.

a) Press "CHAN". "CHAN" switch will light and the CHAN and FREQUENCY displays will clear, ready for entry from the keypad.

b) Select desired channel number (channels 1 through 9 preceded by 0). The display will now flash and allow verification of data stored in that channel. This is a channel recall feature that allows successive number entries to display data (frequency, BFO, and mode information stored in the associated channels).

c) Pressing "E" (enter) tunes the receiver to the last channel recalled. Pressing "C" (clear) returns the receiver to the previously tuned channel.

d) To store or change stored data in a channel, the channel number is recalled per step (b). Then controls are operated to enter frequency, BFO, mode, AGC, or filter in any order by "writing" over previous data. A final "E" (enter) will extinguish the CHAN light indicating data is stored in that channel. Press the FREQ switch. The FREQUENCY display will clear to allow entry of new frequency information. When the frequency has been selected the display will flash to indicate that displayed data does not correspond to the actual operating frequency and also to allow verification of frequency before entry into memory.

To correct an erroneous entry, press "C" and re-enter data. BFO, mode, AGC, and filter switches may be pressed in any order. The data, as displayed by LED readouts or key-lights, is stored when the final "E" (enter) is pressed. The CHAN switch-light will go out and the display will stop flashing to indicate that the programming cycle is completed. The receiver is now tuned to the displayed (and stored) data.

e) Repeat the above procedure to program additional channels - up to 99 available.

3.5.3 FREQUENCY PROGRAM MODE OF OPERATION

The frequency program mode of operation is used to transfer displayed data into a channel. This mode is entered by pressing the FREQ switch first with a succession of optional changes in frequency, BFO, mode, AGC, filter and channel assignment (in any order) followed by pressing "E" to store the selected data in the channel assigned. If no channel is specifically assigned, the data will be stored in a "scratchpad" channel 00.

To change data from one channel (XX) to another (YY): press "CHAN", "XX", and "E" (enter) to tune and display data from channel "XX". Then press "FREQ", "CHAN", "YY" and "E" (enter) to store displayed data into channel "YY".

The following are general step by step instructions for frequency program operation:

a) Press "FREQ". The frequency display will blank and the channel display will read 00.

b) Press up to 7 digits frequency starting with 10 MHz digit. If no digits are entered the frequency will remain as previously selected and will be re-displayed as the next key is pressed. If less than 7 digits of the frequency are pressed, 0's are filled in as the next function is selected. Remaining data (BFO, mode, filter, and AGC) may be entered in any order. Pressing "C" at any time will restore receiver to previous display prior to entering frequency mode.

c) Press "CHAN". Press desired channel number "XX" (channel 1-9 preceded by 0). (Previous channel "XX" data is not recalled as in channel mode).

d) Press desired mode, AGC decay rate or filter switches.

e) Enter BFO offset: press "BFO" (display blanks, switch lights). Enter 0-3 digits. Three digits will complete BFO entry and exit BFO mode. Pressing "E" after incomplete entry will enter trailing 0's and exit BFO mode. Pressing "C" (same as BFO center) will enter all 0's and exit BFO mode. Negative BFO offsets may be entered by pressing BFO twice in succession with an (-) prefix showing in the BFO display. BFO frequency may also be entered by the tune knob (after pressing BFO) and completed by pressing "E".

f) Frequency mode is completed by pressing "E" which enters all the displayed data into the designated channel and extinguishes the FREQ switch-light.

3.5.4 TO PROGRAM BLOCKS OF CHANNELS FOR AUTOMATIC SCAN

a) Press "SCAN PROG". The "SCAN PROG" switch LED will light and the frequency display will go blank, ready for entry from the keypad.

b) Enter the number 1-6 for the block of channels to be scanned.

c) Enter the start (first) and stop (last) channel in the block of channels. A maximum of 99 channels may be entered into any one block.

d) Frequency display indicates block number, start channel and stop channel as entered; example (15 - 66).

e) Repeat above procedure to program additional blocks of channels to be scanned - up to 6 blocks of 99 channels each are available to be scanned.

f) Press "E" (enter) keybutton to terminate scan program mode and enter scan programmed information into memory.

3.5.5 CHANNEL SCAN

a) Press "SCAN ON/OFF". The "SCAN ON/OFF" switch LED will light and the frequency display will go blank, ready for entry from the keypad.

b) Enter the block number (1-6) of the first block of channels to be scanned.

c) Frequency display indicates the block number, start channel and stop channel as stored in memory for block number chosen; example (15 - 66).

d) Enter second block number, for channels to be scanned and repeat for a maximum of 6 blocks. Block numbers may be entered in any order desired.

e) If no block numbers are specified to be scanned, all blocks stored in memory will be scanned.

f) Press "E" (enter) to start the scanning of blocks selected.

g) The scan rate is adjustable by means of a screwdriver adjustment located under the "SCAN PROG" switch located on the front panel.

h) The channel scan sequence may be stopped at anytime by pressing the "SCAN ON/OFF" switch.

i) The channel scan sequence may also be stopped by the presence of a received signal (above a preset audio level) on any of the channels being scanned. The receiver will remain on the channel, where a signal is present, for a period of time determined by a preset internal adjustment. (See Figure 3.3).

j) The channel scan sequence may be restarted by pressing "E".

k) To exit the scan mode, press the "SCAN ON/OFF" switch twice in succession.

Table 3-1
Load Memory Summary

(TABLES FOR LOADING MEMORY)

FOR CHANNEL OPERATION:

1. Press "CHAN"; display clears, "CHAN" LED on.
2. Enter Channel number (single digit channels are preceded by 0).
3. Display will flash; if another channel is desired, it may be re-entered at this time; if already programmed, FREQ information will be displayed.
4. Press "FREQ"; frequency display clears, "FREQ" LED on.
5. ENTER FREQUENCY; display flashes when FREQUENCY display is full; enter BFO, MODE of operation, AGC decay rate, and IF filter as desired.
6. Press "E" to ENTER the CHAN/FREQ information into memory; if the previous display is desired, press "C" to CLEAR the entry and restore former display.

FOR FREQUENCY OPERATION:

1. Press "FREQ"; CHAN display shows "00", frequency display clears, "FREQ" button LED is on.
2. Select desired frequency, BFO, MODE, AGC or filter information as desired.
3. Press "CHAN"; CHAN display clears and frequency display will re-appear, enter channel number.
4. Press "E" to ENTER frequency or "C" to CLEAR the display and restore the previous program.

TO CHANGE MEMORY:

1. Press "FREQ"; CHAN display shows "00", frequency display clears, "FREQ" LED is on.
2. Change any frequency, BFO, mode, AGC or filter information as required.
3. Press "CHAN"; CHAN display clears, frequency display will re-appear, enter channel number.
4. Press "E" to ENTER the CHAN/FREQ information into memory; if the previous display is desired, press "C" to CLEAR the entry and restore former display.

Table 3-1

Load Memory Summary

(Continued)

TO PROGRAM BLOCKS FOR CHANNEL SCAN:

1. Press "SCAN PROG": display clears, "PROG" LED on.
2. Enter number for block of channels to be scanned. (1-6)
3. Enter the channel number (01-99) of the first and last channels to be scanned in the block. (Single digit numbers are preceded by 0).
4. Repeat above procedure for any additional blocks (max. of 6) to be scanned.
5. Press "E" to ENTER block of channels to scanned or "C" to CLEAR the display and restore the previous program.

TO SELECT BLOCKS FOR CHANNEL SCAN:

1. Press "SCAN ON/OFF": display clears, "ON/OFF" LED on.
2. Enter block number of first block of channels to be scanned: Frequency display shows block number, start and stop channels. If no block numbers are specified, all blocks stored in memory will be scanned.
3. Enter additional block numbers to be scanned as required.
4. Press "E" to start the scanning of blocks selected or "C" to CLEAR the display and restore previous receiver status.
5. Press "ON/OFF" to manually stop. Press "E" to resume scanning.
6. Scan will also be stopped for a preset delay time by a signal presence on a channel. Scan will resume after delay time.
7. Pressing "ON/OFF" twice in succession will exit scan mode and return to previous status.

SECTION 4
FUNCTIONAL DESCRIPTIONS

4.1 GENERAL

The MSR 5050 is a modularized state of the art SSB HF communications receiver. The information contained in this section describes the major functions of the receiver. The discussions of the functional descriptions of the receiver will be presented in twelve parts. Each part will contain a discussion of the major functional elements of that part. For a detailed circuit description of a particular part, refer to Section 5 of this manual.

Figure 4.1 shows an overall block diagram of the receiver. Refer to this diagram as the function of each section is described.

4.2 LOW PASS FILTER BOARD, 1A20

The Low Pass Filter board is a plug-in assembly which acts in conjunction with the High Pass Filter board to produce a octave bandpass response which covers the 30 MHz tuning range in 8 bands. Each band is automatically switched by processor control for the frequency being received. The Low Pass Filter contains in series: a 10 watt input protection circuit, a 30 MHz low pass filter and a parallel bank of 8 selectable low pass filters with cut off frequencies of 2, 3, 4, 6, 9, 13 and 30 MHz. The output of the succeeding High Pass Filter is returned to the Low Pass Filter by a bypass switch before going to the mixer board. This switch bypasses the HP Filter in band 1 to allow a response of 10 kHz to 2 MHz.

4.3 HIGH PASS FILTER BOARD, 1A18

This assembly is a plug-in board common to the MSR 8000 transceiver and MSR 6700 exciter which has transmit and receive path functions. In the MSR 5050 receiver it is used for RF amplification and preselection. Contained on this assembly are eight (8) elliptical high pass filters with cutoff frequencies of 1.6, 2, 3, 4, 6, 9, 13 and 20 MHz. The desired filter is selected automatically by ground signals from the interface board, 1A1.

This board also contains a broadcast filter which provides attenuation of greater than 70 dB to broadcast signals (below 1.6 MHz), and a very low noise receive RF amplifier.

4.4 MIXER BOARD, 1A16

The mixer board is a plug-in assembly common to the MSR 8000 transceiver and MSR 6700 exciter which performs all the major frequency conversions in the MSR 5050 receiver. Signals from the low pass filter (.01 to 29.9999 MHz) are applied to a high dynamic range double balanced mixer. The received signal is mixed with the first LO signal (59.63 to 89.53 MHz) from the major loop board, 1A17 (part of the synthesizer) to produce a first IF frequency of 59.53 MHz. The signal then passes through a monolithic crystal filter, a low noise FET amplifier and a second 59.53 MHz monolithic filter before being

applied to a second double balanced mixer. In this mixer the 54.53 MHz second local oscillator from the translator loop board, 1A15 (part of the synthesizer) issued to produce the 5MHz second IF signal. This signal is buffered by FET amplifier Q4 and Q5 (on the mother board) with just enough gain to maintain signal to noise as the signal is sent to the IF filter board, 1A14 (and to 1A12 with ISB or filter options). Other circuits on the mixer board, used in transmit on the MSR 8000 and MSR 6700, are unused in the MSR 5050.

4.5 IF FILTER BOARD, 1A14 (1A12)

The standard MSR 5050 receiver contains one IF filter board, 1A14, which is a plug-in assembly common to the MSR 8000 transceiver and MSR 6700 exciter. This board contains three 5 MHz information filters: FL1 (USB), FL2 (LSB) and FL3 (AM wide). The appropriate filter is selected by diode switching via filter or mode control signals from the interface board, 1A1. The identical board is used with various filters to allow up to six bandwidths or optional ISB mode capability. For ISB mode capability, a second IF filter board, 1A12 is used with the LSB filter positioned in FL1. In radios with ISB option, when ISB is activated, FL1 of 1A12 (LSB) and FL1 of 1A14 (USB) simultaneously selected and produce 2 independent IF paths: IF filter #1 (1A14) to audio squelch #1 (1A10) in the main channel and audio filter #2 (1A12) to audio squelch #2 in the ISB channel. FET switches Q1 and Q2 (on the mother board) are closed and open respectively to steer the signals as required. For a filter option to allow the maximum number of filters, 1A12 is populated with an LSB filter in FL1, a 1 kHz bandwidth (NAR) filter in FL2 and a 400 Hz bandwidth (VNAR) filter in FL3. In addition, IF filter board #1 (1A14) is modified to replace the LSB filter in FL2 to a 12 kHz (VWIDE) filter. When 1A12 and 1A14 filter boards are used, the LSB control signal activates FL1 in 1A12 and the VWIDE control signal activates FL2 in 1A14.

The 5 MHz second IF signal from the mixer board via Q5 (or Q4) is passed through the appropriate IF filter and further amplified in 3 stages. The gain of the IF output is adjustable. An AGC voltage is applied from the audio squelch board (1A10) to two of the amplifier stages to reduce the IF gain on strong received signals. In ISB, the AGC path from 1A10 to the ISB IF filter board (1A12) is broken by a mother board FET switch and replaced by an independent AGC signal from the ISB audio squelch board (1A8).

Transmit circuits on the IF filter board are left unused in the MSR 5050 receiver.

4.6 AUDIO/SQUELCH BOARD, 1A10 (1A8)

The audio/squelch board is a plug-in assembly common to the MSR 8000 transceiver. To provide a second independent channel with the ISB option, a second identical audio/squelch board is plugged into the 1A8 position. The audio squelch board accepts the 5 MHz signal from the IF filter board, 1A14 (or 1A12) and performs the final detection function to convert the IF signal into usable intelligence in the audio frequency range. This process involves two discrete but not simultaneous detector functions. A product detector is used in all modes except AM (where an envelope detector is used) and FM (where a

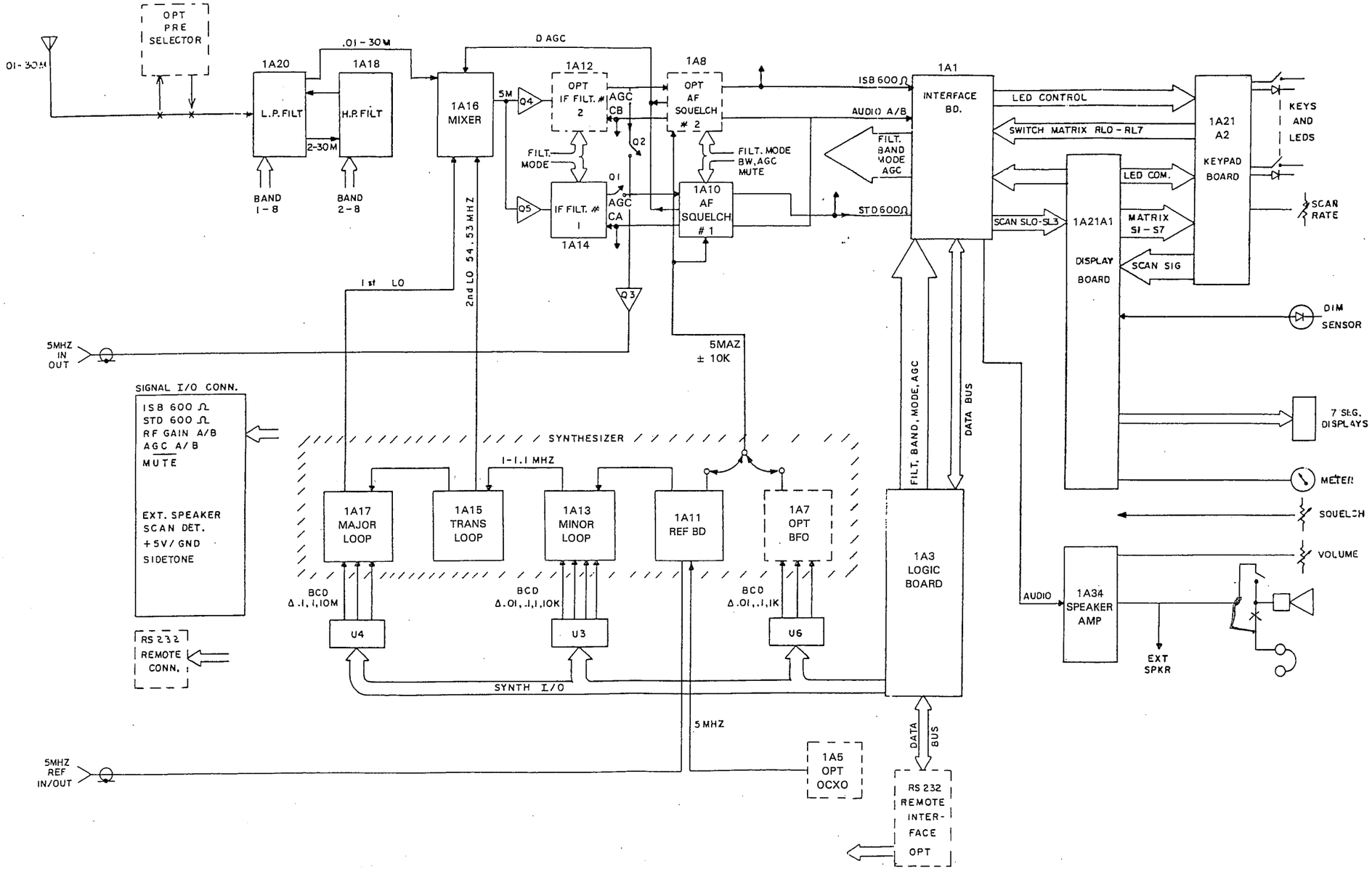


Figure 4.1 Functional Block Diagram

quadrature detector is used) in a separate FM plug-in assembly, using an IF signal taken from the IF filter board, 1A14.

Two separate audio outputs are provided. A 600 ohm line audio output is applied to the rear panel connector, J42 and to the meter circuit via the interface board, 1A1. A low level output is developed to drive the speaker amplifier board, 1A34, via switching circuitry in the interface board, 1A1 and display board 1A21A1, to provide the front panel speaker and headphone audio.

Located on this board are an input amplifier, AGC detector and amplifier, AM/product detector, squelch amplifier and gating circuitry. In the AM mode, AGC is carrier derived. In CW, SSB and FSK modes, AGC is derived from the detected audio. Fast attack is used in all modes. Externally switched decay resistors allow front panel selection of fast, medium or slow AGC decay rates. The AGC voltage to the IF filter board, 1A14 (or 1A12) and delayed AGC voltage (DAGC) to the mixer board, 1A16, controls the receiver gain and goes to the front panel signal strength meter via circuitry in the interface board, 1A1 and display board, 1A21A1. The AGC voltage output and an AGC over-ride input line is brought to the rear panel connector for diversity applications.

Other circuitry allows adjustment of squelch threshold (front panel) and mute (rear panel) of speaker audio. A side tone input allows external audio (rear panel) or FM audio (with (with optional FM board) to be inserted in the speaker audio signal path.

4.7 INTERFACE BOARD, 1A1

The interface board is a plug-in assembly which serves mainly as an interconnect between the front panel assembly, 1A21 and the motherboard, 1A2. Connection to the front panel assembly is by three ribbon cable connectors.

Circuitry is contained to control the 34 front panel matrix-organized switches and 16 seven-segment displays with communication to the logic board, 1A3, microprocessor via an 8 bit data buss.

Coded signals from the logic board, 1A3, for band, mode, filter and AGC selection are decoded to drive switch indicator LED's on the front panel keypad board, 1A21A2 and to control switch functions in associated assemblies.

Circuitry is contained which converts the dc voltage from the front panel tuning control to variable rate pulses, on two lines, to the logic board microprocessor which step the frequency (or BFO offset) up or down.

Other circuitry on the board includes audio meter detectors; channel scan oscillator, delay and detector circuits and a D-to-A/A-to-D converter to provide remote meter indications.

The same interface board is used in the MSR 6406 remote control unit with similar functions. The decoded band, filter, etc. control signals are unused and only indicate the status of the controlled receiver. The D-to-A/A-to-D converter is jumpered to perform a D-to-A conversion of digital RF meter level.

4.8 LOGIC BOARD, 1A3

The logic board is used in the MSR 5050 receiver and it's remote control unit MSR 6406 as well as the MSR 6700 exciter and its remote control unit MSR 6404. The only difference in the boards, identified by group number, is in the programming contained in two plug-in program memory chips (U4 and U15).

This board contains the microprocessor and supporting circuitry to supply frequency, band, mode, filter, AGC speed, BFO offset and channel information to assemblies in the receiver. Similar functions are controlled in the exciter. Program memory is stored in two 2K x 8 EPROMS. Channel data storage for 99 channels of frequency, channel number, band, AGC speed, mode and filter data is contained in two 1K x 4 bit RAM's. A lithium battery provides a keep-alive voltage to maintain memory when not powered externally. A priority interrupt chip, I/O expanders and gates interface the microprocessor with external control inputs and outputs in the system.

4.9 FRONT PANEL ASSEMBLY, 1A21

The front panel assembly contains all controls and indicators for operating the MSR 5050 receiver. Mounted to the front panel are the display board, keypad board, speaker, phone jack and controls for volume/power-on, squelch and speaker on/off. The front panel assembly is connected to the receiver by 4 nuts, 3 screws and 4 ribbon cable connectors.

4.9.1 DISPLAY BOARD, 1A21A1

The display board mounts to the front panel and connects to the interface board and keypad board by ribbon cable connectors. It receives its signals from the interface board to display channel, frequency, emission mode, bite, radio set and BFO in 16 seven-segment LED displays on the front panel.

Also contained is the meter and associated switching circuitry to indicate RF and audio signal levels. Voltage regulator circuitry for the displays on the display board as well as the switch LED indicators on the keypad board, is controlled by a photocell to provide an ambient light adaptive dimmer.

The tuning control, spring loaded to center, is also contained on the display board. It provides a dc voltage, proportional to rotation angle, to the interface board. This voltage is converted to up or down tuning pulses to the logic board.

4.9.2 KEYPAD BOARD, A21A2

The keypad board mounts to the front panel and connects to the display board and interface board with ribbon cable connectors. The front panel board contains 34 momentary switches, arranged in a matrix. These switches generate signals to the keypad chip in the interface board, which communicate key closure data to the logic board via an 8 bit data buss. Other switches control switching circuitry in the display board to direct audio or RF level signals to the meter and speaker.

All but the numeric 0 through 9 pushbutton switches, contain LED indicators, driven from the logic board (or switching circuits), which indicate that the key closure has been executed. The Keypad board also contains the scan rate adjustment pot and a decoder to produce the 6 scan lines in the switch matrix.

4.10 SPEAKER AMPLIFIER, 1A34

The speaker amplifier is a plug-in board containing an integrated circuit with circuitry to provide 4 watts to drive the speaker. The input is generated in the audio squelch board. With the ISB option the input may come from either the standard or ISB audio squelch board as selected by switching circuits on the display board in response to USB or LSB monitor switches. After the audio source is selected, the volume control directly controls the input to the board. The output of the speaker amplifier board drives the speaker and headphone jack and is also available on the rear panel signal in/out jack, J42.

4.11 FREQUENCY SYNTHESIZER, 1A9, 1A11, 1A13, 1A15 (1A7)

The frequency synthesizer consists of normally 4 subassemblies: reference board, minor loop board, translator loop board and the major loop board. The synthesizer provides the three local oscillator signals that determine the operating frequency of the receiver. These signals are obtained from the 5 MHz reference oscillator directly and by a combination of direct synthesis and digital phase lock techniques. Frequency accuracy is dependent only on the 5 MHz TCXO oscillator on the reference board (or external TTL 5 MHz reference via the rear panel as desired). With the BFO option, the BFO board provides a variable 3rd LO in place of the fixed 5 MHz from the reference board.

4.11.1 REFERENCE BOARD, 1A9

The reference board contains a 5 MHz TCXO which is used to drive a 1 kHz reference to drive the minor loop board and BFO board. A 50 kHz reference is also generated to drive the major loop board and a 5 MHz filtered sine wave to derive the product detector in the audio squelch board. Tristate buffers and a jumper allow an external 5 MHz signal to drive the reference board in place of the TCXO. Also developed on the board, is a 24 volt power supply which is used in the major loop board.

4.11.2 MINOR LOOP BOARD, 1A11

This assembly supplies the 1.0 to 1.09999 MHz signal to the translator loop board, 1A13, which determines the 10 Hz, 100 Hz, 1 kHz and 10 kHz digits of the receiver frequency. Inputs to this board are a 1 kHz reference signal from the reference board, 1A9 and the 10 Hz, 100 Hz, 1 kHz and 10 kHz BCD inputs from the 8243 I/O expander (U2) on the mother board which is directed by the logic board microprocessor.

4.11.3 TRANSLATOR LOOP BOARD, 1A13

The translator loop board provides the 54.53 MHz second LO, which is applied to the mixer board. This signal originates from a crystal oscillator and is not referenced to

the frequency standard, therefore a small frequency error can exist in the second LO. Due to the mixing scheme used in this assembly, the same error appears on the first LO at the output of the first mixer board. This board supplies to the major loop board, a 55.53-55.62999 MHz signal. This signal is essentially a mixture of the low digit signal 1-1.09999 MHz and the second LO (54.53 MHz including frequency error).

4.11.4 MAJOR LOOP BOARD, 1A15

The major loop board supplies the first LO signal (59.53-89.53 MHz) to the mixer board. The first LO is a phase locked oscillator covering the frequency range of 59.53000 MHz to 89.52999 MHz, in 10 Hz steps. The exact frequency of the first LO is given by:

F1 = 59.53000 + Fd + e (MHz)

where F1 = first LO frequency
Fd = dialed frequency
e = second LO error

The first LO is used to convert the incoming signal up to the first IF frequency (59.53 MHz).

This board determines the 10 MHz, 1 MHz and 100 kHz digits of the receiver frequency. Inputs to this board are the 55.53-55.62999 MHz signal from the translator loop board, a 50 kHz signal and +24 VDC from the reference board, and 10 MHz, 1 MHz and 100 kHz BCD inputs from the 8243 I/O expander (U3) on the mother board as directed by the logic board microprocessor.

4.11.5 BFO BOARD, 1A7 (OPTION)

The BFO board is a plug-in option that provides a reference-locked synthesized third LO which replaces that from the reference board (by a mother board jumper). It provides a $\pm$ 7.99 kHz offset in 10 Hz steps by varying the output above and below 5 MHz. Because of the frequency inversion in the receiver, a BFO output above 5 MHz is actually a minus offset referred to incoming signals. The BCD word for absolute value of offset is used in the microprocessor with a sign indicating offset direction. With frequencies below 5 MHz (+offset) the microprocessor outputs the BCD word to drive the BFO display. It performs a logical subtraction of the BCD word from 10K and the result drives the BCD inputs of the board via the 8243 I/O expander (U4) on the mother board. A bit representing the sign causes 10K to be subtracted from the preset inputs thus resulting in a frequency of 5 MHz-BCD data.

A disable input allows the 5 MHz output to be disabled on the board for AM or FM applications where the signal could interfere with normal signal processing.

4.12 REAR PANEL ASSEMBLY, 1A22

The rear panel assembly contains the power supply assembly 1A22A1 and external signal and power interface connectors. The ac line voltage connector 1A22J40 has a built-in line filter, fuse holder and line voltage switch card. Coax connectors are provided for antenna input J46, IF monitor output J45 and reference in/out J41. The IF monitor output is a sample of the 5 MHz

second IF signal after filtering in the IF filter board. The reference in/out connector either outputs the buffered TCXO TTL signal on the reference board, 1A9 or accepts external TTL 5 MHz inputs to replace the TCXO as determined by the position of the REF switch S1 adjacent to the connector. A 25 pin "D" connector, J42, provides line audio and speaker outputs, remote control signals for current loop and FSK control, and miscellaneous signals such as AGC, RF gain, mute and scan detector. The rear panel is removeable by 9 screws, 3 molex connectors, 3 coax connectors and a ribbon cable connector. Provisions are made for connectors J43 and J44 for remote control options via RS232 or IEEE-488.

4.12.1.1 POWER SUPPLY BOARD, 1A22A1A1

The power supply board contains regulators for the 5, 9 and 13 volt outputs. The pass transistors for each regulator are in sockets on the heat-sink to which the power supply board is mounted and are accessable and removeable from the rear panel. The 9 and 13 volt regulators operate from a 16 volt rectified input while the 5 volt regulator operates from a separate 10 volt input. The power on/off function for the receiver is provided by a dc ground from the front panel volume/power-on control which enables all three regulators.

Voltage detectors activate LED indicators visible from the top of the board to show presence of each regulated voltage. A separate detector provides a TTL low output when the 9 or 13 volts are below tolerance. This signal is fed to the logic board to indicate a code E2 on the front panel BITE display. The 5 volt regulator is adjustable. The regulators are designed to operate from a nominal line voltage $\pm$ 15 percent.

A 13 volt supply for an optional oven controlled reference oscillator is provided by "OR"ing the regulated 13 volts with a preregulator-derived voltage which is always present.

4.13 MOTHER BOARD, 1A2

The mother board is a 1/8 inch PC board which serves mainly as a signal interconnection between twenty plug-in PC boards, a rear panel assembly and a front panel assembly. The board is also used to enforce the mechanical stability of the chassis and to complete the shielding integrity of the metal "card cage" around the signal path and synthesizer boards.

I/O expanders are mounted in sockets, controlled by the logic board microprocessor to provide frequency inputs to the BFO board (by U6), to the minor loop board (by U3) and to the major loop board (by U4). Option enables jumpers to U4, alter the microprocessor program to activate indicators and controls for the option desired. FET buffer amplifiers Q4 and Q5 boost the 5 MHz mixer IF output signal to maintain signal-to-noise while providing two isolated signal paths to the IF filter boards. FET switches Q1 and Q2 divert IF signals from the IF filter boards to the appropriate audio squelch board as directed by logic circuits, depending on the filter or mode selected.

SECTION 5
MAINTENANCE

5.1 GENERAL

This section provides information for routine maintenance, repair and evaluation of the overall performance of the receiver. Modular construction of the receiver lends itself to a logical and straight forward troubleshooting procedure. By referring to the overall and individual block diagrams, and using related level and frequency information, a trouble can be quickly localized to a particular assembly. Voltage and signal levels to all assemblies, except the rear panel 1A22, and front panel, 1A21, may be measured on the mother board, 1A2, at the appropriate connector or signal point.

After establishing the existance of a trouble in a particular assembly, refer to the servicing information for that assembly located elsewhere in this section of the manual.

Figure 5.1 locates the component assemblies in the receiver and Figure 5.2 shows the locations for those assemblies from the bottom side of the receiver.

5.2 PC BOARD REPAIRS

5.2.1 REMOVAL AND REINSTALLATION

Care should be used when removing PC boards from the transceiver. The card extractor, P/N 600268-618-001, should be used if possible. If no card extractor is available, a temporary substitute can be made from a length of solid heavy guage wire (#10-#12). Form a hook at each end of the wire, and then insert each hook into the holes provided at the top outer edge of each PC board. Apply gentle upward pressure near each hook to free the board(s) from their edge connectors.

NOTE

DO NOT USE PLIERS OR SCREWDRIVERS TO REMOVE THE BOARDS.

When replacing boards into the PC sockets, insure that the board is in its proper position in the card guides at each board edge. Apply light downward pressure to the top edge of the board until it is fully seated into its edge connector.

5.2.2 SOLDERING

To avoid damaging the PC boards during the replacement of components, extreme care should be used in soldering and component removal. A low wattage soldering iron (25-50 watts) with a narrow tip should be used.

A low wattage iron is necessary to prevent the application of excessive heat to the copper foil of the PC board. Excessive heat may cause the foil to separate from the board, rendering the board unrepairable. Only a high quality electronic grade rosin solder should be used in making repairs.

CAUTION

DO NOT USE AN ACID CORE SOLDER.

Due to the circuit density on the boards, solder "bridges" or short circuits between adjacent foil runs are possible, if care is not used during soldering operations. After

soldering is completed, the area around the connection should be closely inspected for excess solder or "bridges" between adjacent runs or connections. Any "bridges" or excess solder between connections must be removed before reinstalling the board. Because of the double sided construction used on the PC boards, a component lead may be soldered to printed circuit areas on top and bottom of the board. Consequently, when a component lead is removed, the replacement component should be resoldered top and bottom as applicable.

5.2.3 CMOS DEVICE HANDLING PRECAUTIONS

CMOS devices may be damaged by static voltages, and therefore the following is recommended:

a) All MOS devices should be placed on a grounded work bench surface, and the repair operator should be grounded prior to handling MOS devices, since a person can be statically charged with respect to the work bench surface.

b) Nylon clothing should not be worn while handling MOS circuit or devices.

c) Do not insert or remove MOS devices from sockets while power is applied.

d) When soldering MOS devices, be sure the soldering iron used is a grounded type.

5.3 LOGIC INTERPRETATION

Several types of digital devices are used in the receiver. The following descriptions are presented to explain their basic operation and symbolic notation. The digital devices used (gates, flip-flops, inverters, etc.) are binary in nature; that is, the output voltage of each can only be in two permissible states. The two possible states are called logic "1" and logic "0". The assignment of voltage levels to these states is arbitrary. However, in this manual positive logic is standarized, which means we define the logic states as shown in Table 5.1.

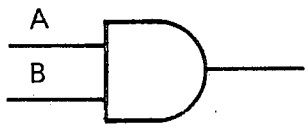
Table 5.1
Logic States

	TTL	CMOS
LOGIC 1: Normally greater than	2.0 Volts	7.0 Volts
LOGIC 0: Normally less than	0.8 Volts	3.0 Volts

5.3.1 GATES

A gate is a circuit element whose output level depends upon the levels of all of its inputs in a particular pattern.

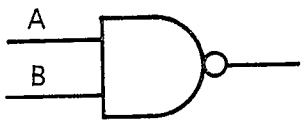
AND GATE



INPUTS		OUTPUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1

The AND gate can have two or more inputs, the level of its output is dependent on the state of all input levels. IT can be seen from the truth table for the AND gate if any input is 0, the output will be 0. For the output to be 1, all inputs must be 1.

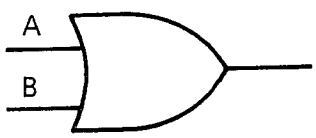
NAND GATE



INPUTS		OUTPUT
A	B	
0	0	1
1	0	1
0	1	1
1	1	0

The outputs of the NAND gate are the opposite of the AND gate. If any input is 0, the output will be 1.

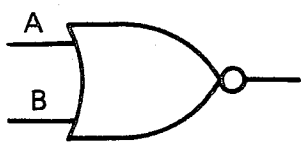
OR GATE



INPUTS		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1

The output of the OR gate is 1 if any input is 1.

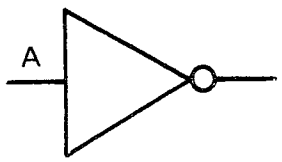
NOR GATE



INPUTS		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

The output of the NOR gate is the opposite of the OR gate. The output is 0 if any input is 1.

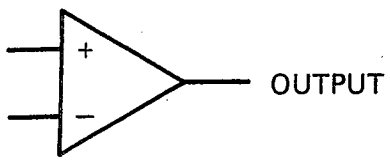
5.3.2 INVERTER



INPUT	OUTPUT
0	1
1	0

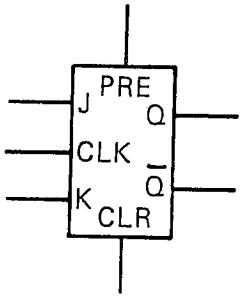
The inverter has a single input. The output level is the opposite of the input level.

5.3.3 VOLTAGE COMPARATOR



The voltage comparator has two inputs, V+ and V-. The V+ input is normally connected to a fixed or reference voltage. The V- input is usually variable. As the V- input becomes more positive and exceeds the V+ input level, the output switches low. If the V- input voltage becomes less positive than the V+ reference input, the output switches to a high level once again.

5.3.4 J-K FLIP-FLOP



The flip-flop is a memory device that stores a logic state. The above symbol is that of a J-K flip-flop. The state of which is referred to by the level of the Q output. If, for example, the Q output is high, the FF (flip-flop) contains a 1. The Q (Q NOT) output is always the opposite of the Q output. The state of the FF can be changed in two ways. It can be changed by means of the clock input, or by the PRESET and CLEAR inputs. The effect of an applied clock pulse on the state of a FF depends upon the J and K inputs. The J input must be high for a clock pulse to cause a 1 output. The K input must be high for a clock pulse to cause a 0 output. If both J and K inputs are high, the FF toggles (changes state) on each applied clock pulse.

The PRESET and CLEAR inputs operate independently of the clock. A high level input to the PRESET line drives the FF to a level 1, while a high input to the CLEAR line drives the FF to a level 0. Some circuits PRESET or CLEAR with a low level input instead of a high level. This is indicated by a "circle" at the appropriate input terminal.

5.3.5 MICROPROCESSOR

The microprocessor is basically a small computer contained within an integrated circuit. This is a device that can store, retrieve, and process data. They are manufactured in many different configurations. The microprocessor, used in this receiver, contains an 8 bit central processor unit, a 64 byte on chip RAM, 27 input/output lines, and an internal clock. It is configured in a 40 pin dual in line package.

5.3.6 INPUT/OUTPUT PORT (8 BIT LATCH)

The input/output port is an interface device for use with a microprocessor. It contains, within one package, a large number of gates, buffers, and flip-flops. They are manufactured in many different configurations. The in/out port used in this receiver is configured in a 24 pin dual in line package.

5.3.7 RAM

Random access memories are logic elements that can be reprogrammed over again many times, and the information stored, can be retrieved by utilizing read/write, and address inputs. 8K bit CMOS RAM's are used in the receiver memory system for reliability and low power consumption. They are configured in a 18 pin dual in line package.

5.3.8 INPUT/OUTPUT EXPANDER

The input/output expander is an interface device for use with a microprocessor. The function of which is

to increase the permissible number of inputs and outputs to the microprocessor. It contains within one package, a large number of buffers, latches, decoders, and other logic circuitry. I/O expanders are used in the logic board and mother board. They are configured in 24 pin dual in line packages.

5.3.9 EPROM

Eprom's are electrically programmable, ultraviolet light erasable data storage devices which control the microprocessor. Two 24-pin 8K bit devices are used in the receiver logic board.

5.3.10 PRIORITY INTERRUPT

This 24-pin device assigns priority to 8 interrupt inputs to control the interrupt to the microprocessor.

5.3.11 TRISTATE BUFFER

A tristate buffer has the normal TTL high and low states plus a controllable off (or open circuit) state which allows bidirectional operation.

5.3.12 PROGRAMMABLE KEYBOARD/ DISPLAY INTERFACE

This 40-pin IC operates with the microprocessor to interface keyboard inputs (up to 8 x 8 matrix) and 16 seven-segment displays.

5.4 ASSEMBLY AND SUBASSEMBLY IDENTIFICATION

Table 5.2 and Figure 5.3 lists and identifies the assemblies and modules used in the transceiver. Figure 5.4 is an interconnection/ wiring diagram for the receiver. Schematics for each assembly and module, parts lists, and circuit descriptions are contained in this chapter of the manual.

Most signal path and synthesizer boards described here are also used in the MSR 8000 transceiver and MSR 6700 exciter and are fully interchangeable. In addition, the MSR 5050 minor loop (with 10 Hz resolution) is interchangeable with the MSR 8000 minor loop (100 Hz resolution). The resulting resolution is limited by the type board used or the unit's controls.

Two versions of reference boards are in use and both are interchangeable within limits. The MSR 5050 reference board has the added capability of either outputting the 5 MHz reference signal or accepting an external signal as determined by a TTL control signal.

5.5 COVER REMOVAL

The top cover is removed by two quarter turn fasteners. The top inner cover can be removed by removing the eight (8) mounting screws that secure the inner cover to the chassis. See Figure 5.5.

The bottom cover is held by 10 screws to the chassis, rear panel and front panel.

5.6 RECEIVER ALIGNMENT AND ADJUSTMENTS

All modules and assemblies of the receiver are of high reliability, solid state design. Adjustments and alignments are seldom, if ever, required. If a module or component replacement or performance indicates the need for adjustment or alignment, the following tables and procedures are provided.

Before performing adjustments, it is recommended that Section 4, Functional Description, and Figure 4.1, the block diagram be reviewed for a more complete understanding of the receiver.

5.6.1 PRELIMINARY ADJUSTMENTS

Before performing adjustments on the receiver:

a) Connect an RF signal generator (HP 8640B or equal) to the antenna connector of the receiver, 1A22J46.

b) Set the generator frequency an output as listed in Table 5.3. See Figures 5.1 and 5.6 for the locations of the modules and adjustments.

c) Audio output may be measured by an audio voltmeter (HP 400LR or equal) connected to the 600 ohm receiver output (1A22J42, pins 24 and 23).

d) To make some of the adjustments on the assemblies, it is necessary to use an extender card (optional equipment, part number 601198-536-001).

Table 5.2

Recommended Test Equipment

2 each, Signal Generators	HP 8640B or equal
Audio Meter and Distortion Analyzer	HP 334A or equal
Frequency Counter	Accurate to 0.1 PPM at 30 MHz
Audio Generators	HP 200CD or equal
Digital Voltmeter	HP 3466A or equal
Spectrum Analyzer	HP 141T with 8553B and 8556A RF sections
Boonton	Model 92C Voltmeter with 91-7C divider or equal
RF Combiner	Merrimac PD-20-10-M2
Power Meter and Load	GR1840 or equal
Oscilloscope	Tektronix 475 or equal
Extender Cards	6.5" wide, 2 each (P/N 601198-536-001)
Signal Input/Output Monitor Fixture	Connections to A22J42 (See Figure 5.41)

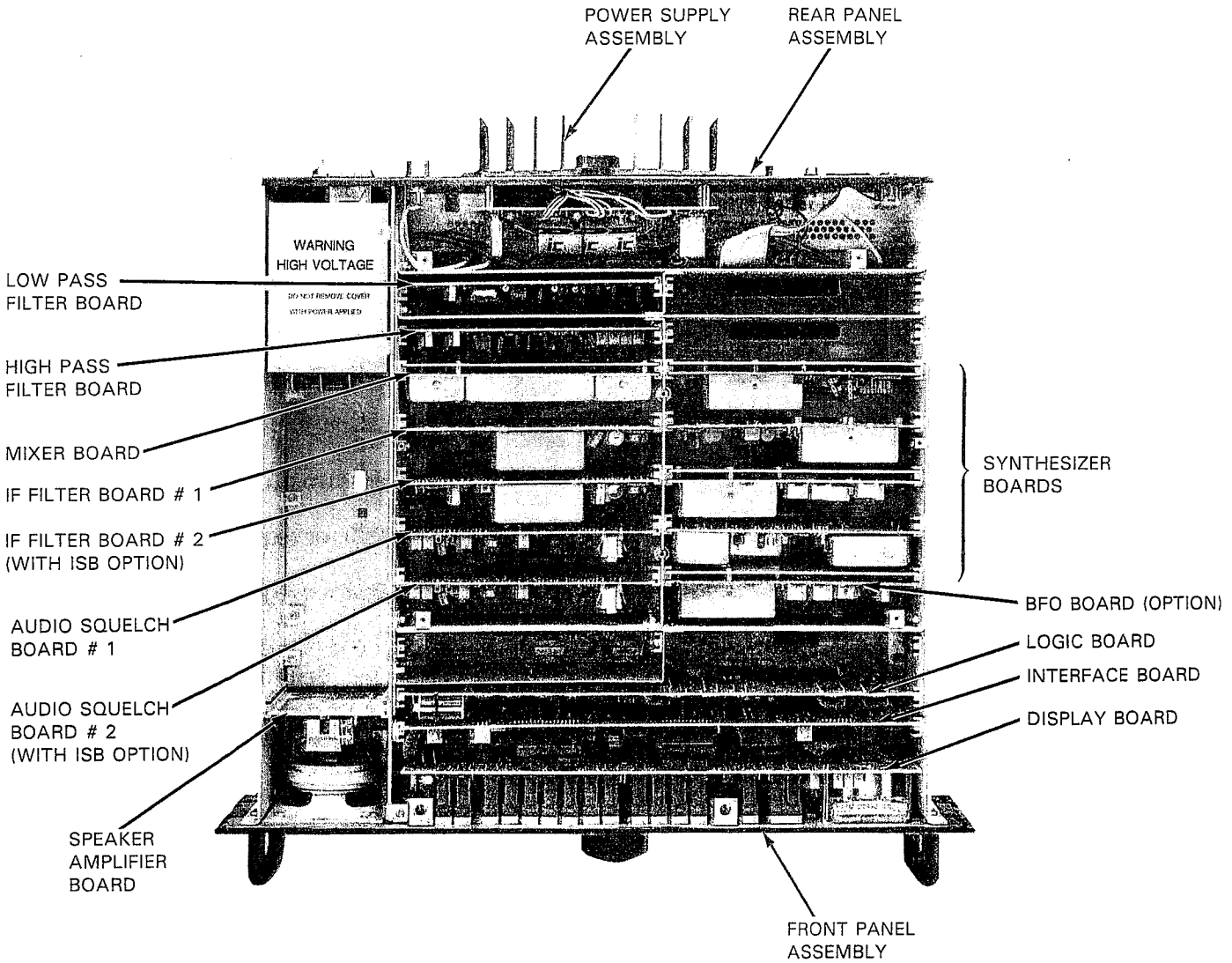
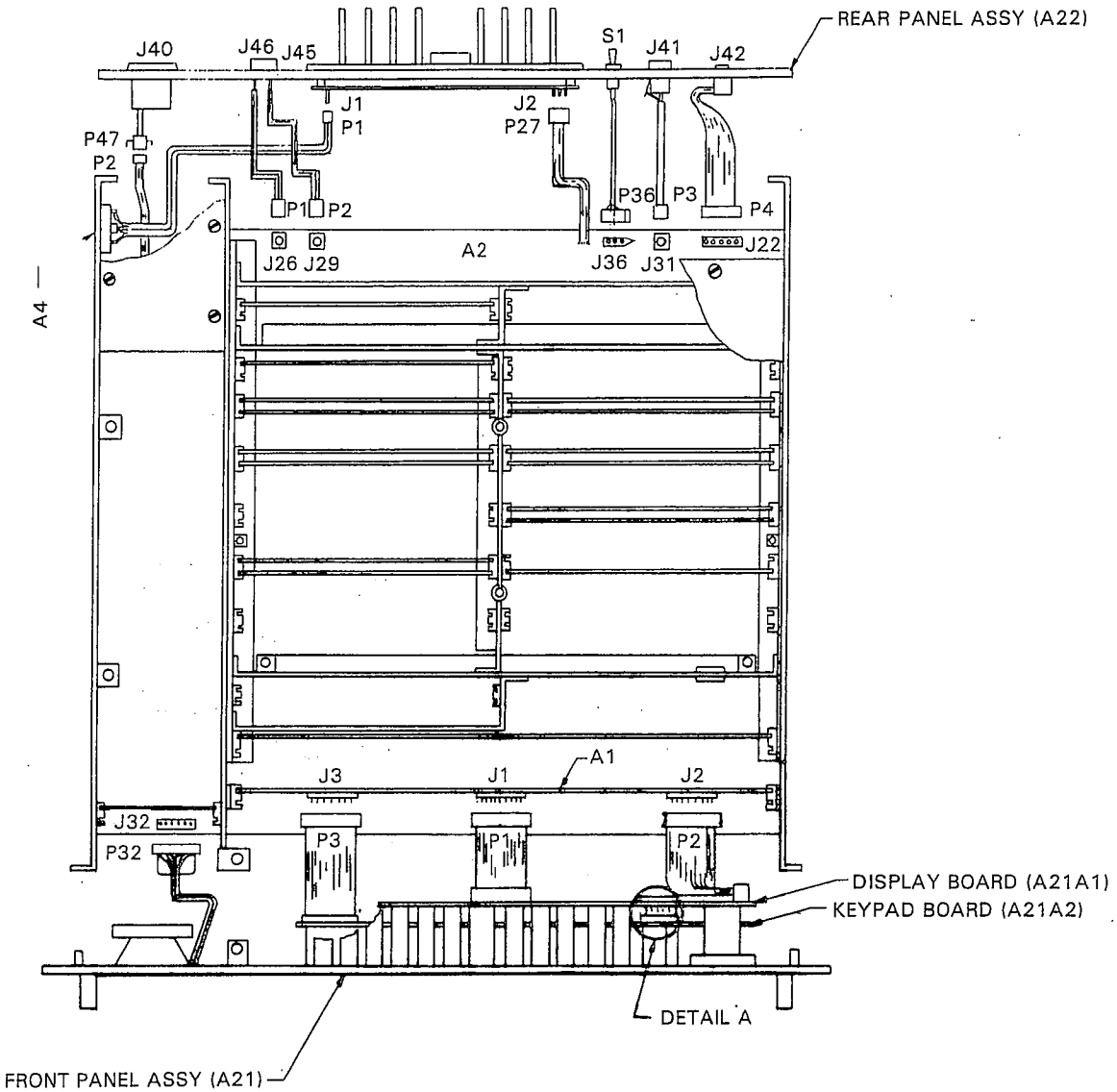
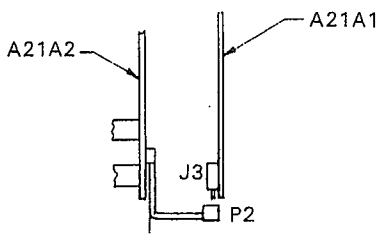


Figure 5.1 Receiver Assemblies





DETAIL A

Figure 5.2 Receiver
Simplified Wiring Diagram

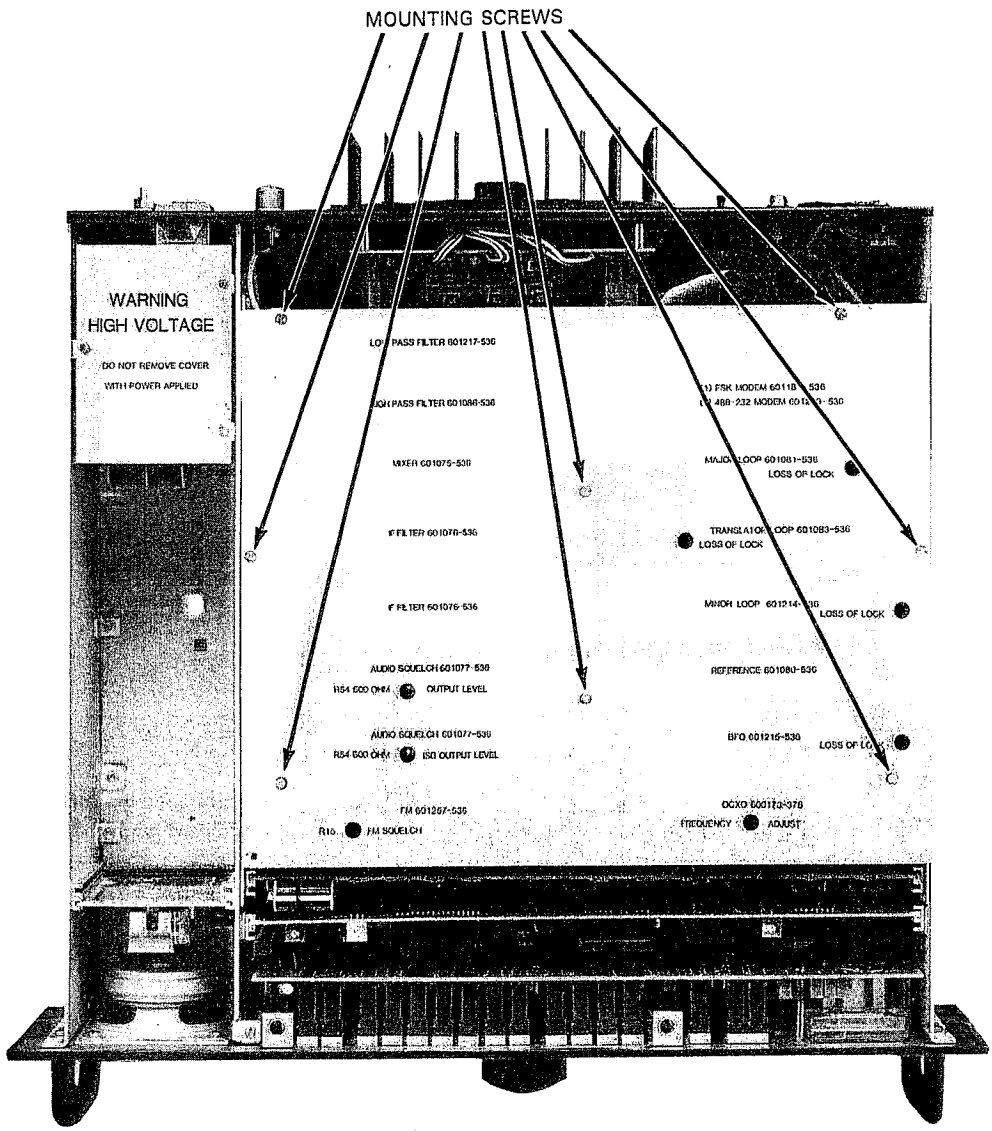


Figure 5.3 Top Shield Mounting Screws

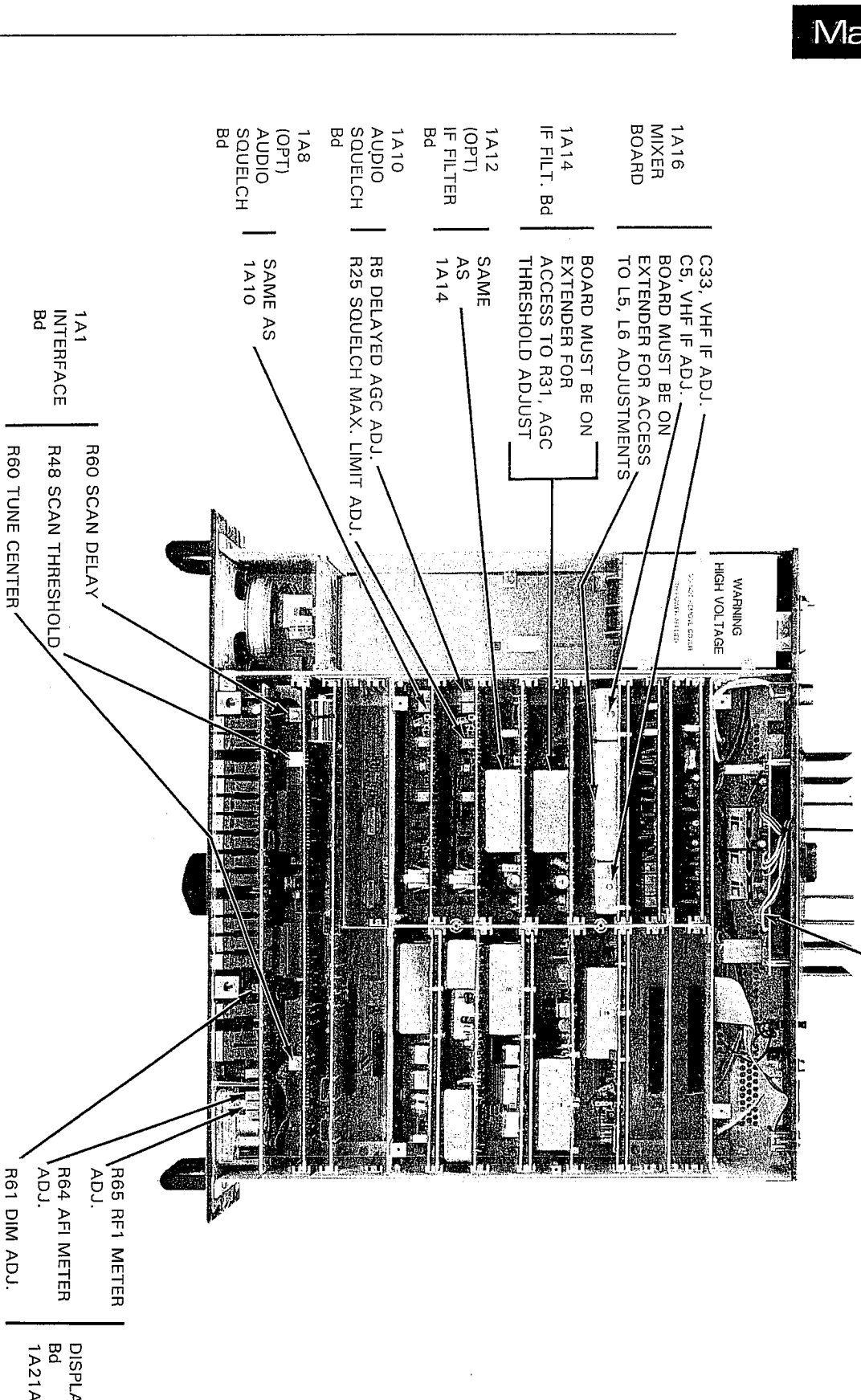


Figure 5.4 Adjustment Locations

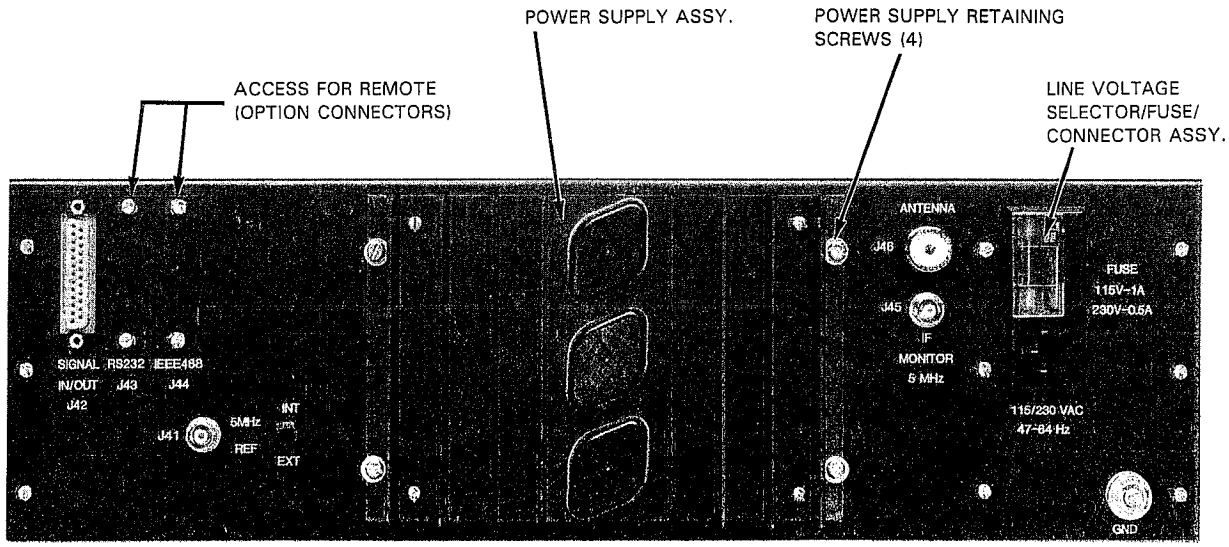


FIGURE 5.5 Rear Panel Components

Table 5.3

Receiver Assemblies

DESIGNATOR ASSEMBLY/SUBASSEMBLY	DESCRIPTION	PART NUMBER
1A1	Receiver Top Assembly	690024-000
1A1A1	Interface Board	601180-536
1A1A2	Mother Board	601212-536
1A1A3	Logic Board	601179-536-001
1A1A4	Chassis Assembly	600424-705
1A1A5	OCXO Assembly (option)	600173-378-001
1A1A6	FM Board (option)	601257-536-001
1A1A7	BFO Board (option)	601215-536-001
1A1A8	Audio Squelch Board (ISB option)	601077-536-003
1A1A9	Reference Board	601080-536
1A1A10	Audio Squelch Board	601072-536-003
1A1A11	Minor Loop Board	601214-536-001
1A1A12	IF Filter Board (ISB option A) (Filter option)	601076-536-002 601076-536-003
1A1A13	Translator Loop Board	601083-536-001
1A1A14	IF Filter Board-Basic Receiver (Filter option)	601076-536-005 601076-536-004
1A1A15	Major Loop Board	601081-536-001
1A1A16	Mixer Board	601075-536-001C
1A1A17	Current Loop/RS232 UART Board (Remote option)	601335-536-001
1A1A18	High Pass Filter Board	601086-536-001
1A1A19	Modem Board (FSK Remote option)	601181-536-001
"	FSK/Audio Modem Board (Voice plus Data Remote option)	601414-536-001
1A1A20	Low Pass Filter Board	601217-536-001
1A1A21	Front Panel Assembly, Grey	600066-539-001
"	Front Panel Assembly, Olive	600066-539-002
1A1A21A1	Display Board	601269-536-001
1A1A21A2	Keypad Board	601225-536-001
1A1A22	Rear Panel Assembly	600069-536-001
1A1A22A1	Power Supply Assembly	600423-705-001
1A1A23	Left Side Support Assembly	600500-706-001
1A1A24	Top Shield Assembly	600265-604-001
1A1A25	Top Cover Assembly	600706-612-001
1A1A34	Speaker Amplifier Board	601311-536-001

Table 5.4

Receiver Adjustments

ASSEMBLY	ADJUSTMENTS AND PERFORMANCE
1A1A22A1 Power Supply Assembly	1) R14 (5 Volt Adj.): Measure dc voltage at rear panel J42-6. Adjust for 5.0 VDC.
1A1A16 Mixer Board	1) C5, C33, L5, L6 (VHF IF Adj: Frequency to 11.6 MHz, mode to USB. Apply 0.5 uV RF, adjust for maximum audio output (>10 dB S+N/N).
1A1A10 Audio Squelch Board	1) R5 (Delay AGC Adj.): Frequency to 11.6 MHz, USB, increase signal to obtain 4.4 VDC at TP1. Adjust R5 for 7 VDC at TP2. 2) R25 (Squelch Max. Threshold Limit Adj.): Front panel squelch control max. CW; apply 20 uV input. Adjust R25 until squelch just "opens".
1A1A21A1 Display Board	1) R65 (RF1 Meter Adj.): Same RF input but level to -7 dBm press "RF" meter switch. Adjust for full scale (+100 dBuV) meter indication. 2) R64 (AF1 Meter Adj): Same input, press "AF" meter switch. Monitor STD 600 ohm output (rear panel 1A22J42 - pin 22/20) and adjust R64 for corresponding meter indication - normally 0 dBm. 3) R61 (Dimmer Adj.): Cover front panel photocell window to the left of the meter. Adjust R61 for barely discernable display intensity.
1A1 Interface Board	1) R42 (Tuning Center Adj.): Monitor TP1 (tuning voltage) should be 2.5 VDC. Adjust R42 to make TP2 voltage (tuning center) equal to TP1. 2) R48 (Scan Threshold): Monitor TP3 - receiver not in scan mode. Adjust R48 for .025 VDC. 3) R60 (Scan Delay): Adjust as desired during scan for .5 to 5 seconds.

Table 5.5

Troubleshooting Chart

ASSEMBLY	ADJUSTMENTS AND PERFORMANCE
1 Receiver inoperative, Display and Key Lights not lit. Power Supply LED's not lit.	1) AC line cord defective or not connected. 2) Fuse blown. 3) Transformer 1A23T1 or Rectifiers 1A23CR1 and 1A23CR2 defective. 4) Cables 1A2P27 or 1A23P1 not plugged into Power Supply 1A22A1. 5) Front Panel Cable 1A21P32 not plugged into mother board. 6) Defective Front Panel Volume Control Power Switch 1A21R2/S2. 7) Defective Power Supply Assembly 1A22A1.
2 No Audio or Background Noise at Speaker or Phone Jack. Meter indicates RF Signal present.	1) Speaker switch off or defective. 2) Volume control at "Min" position or defective. 3) Squelch control at "Max" full clockwise position. 4) Defective Cable 1A21 P32. 5) Defective Speaker Amplifier Board 1A34. 6) Defective Audio Squelch Board 1A10. 7) Defective Interface Board 1A1. 8) Defective Display Board 1A21A1. 9) Display Board Cable 1A21A1 P2 not connected or improperly connected to interface board. 10) Ground on Mother Board "LL" trace or $\overline{\text{Mute}}$ Line or Rear Panel Connection 1A22J42, pin 20.
3 Same but Meter may or may not indicate. One of the Synthesizer "Loss of Lock" lights indicating.	1) Defective Synthesizer Board 1A11, 1A13, 1A15, 1A17 or optional 1A7. (Remove top cover and locate defective board by illuminated loss-lock LED.)

Table 5.5
(continued)

ASSEMBLY	ADJUSTMENTS AND PERFORMANCE
4 AM Mode normal; other Modes inoperative (check AM-Wide and AM-Medium).	1) 3rd LO injection absent at Audio Squelch Board 1A10. a. Mother Board Jumpers JP4, JP5 or JP6 incorrectly placed. b. Defective Reference Board 1A11 (or option BFO Board 1A7). 2) Defective Logic Board 1A3. 3) Defective Interface Board 1A1.
5 Distorted Audio at Speaker.	1) Defective Speaker Amplifier Board 1A34. 2) Defective Audio Squelch Board 1A10. 3) Defective Interface Board 1A1. 4) Defective Display Board 1A21A1.
6 Receiver Signals weak in all Modes. "S" Meter indicates low.	1) Defective High Pass Filter Board 1A20. 2) Defective Low Pass Filter Board 1A18. 3) Defective Mixer Board 1A16. 4) Defective IF Filter Board 1A14. 5) Defective Rear Panel Cable 1A22P4 to mother board. 6) Defective Mother Board Buffer Amplifier 1A2Q4. 7) Defective Audio Squelch Board (i.e. DAGC pot adjusted too "early"). 8) Defective Logic Board (band A, B, C code incorrect). 9) Defective Interface Board (band 1 through 8 signals incorrect).
7 Received Signals weak in some but not all Bands.	1) Defective Low Pass Filter Board 1A18. 2) Defective High Pass Filter Board 1A20. 3) Defective Logic Board 1A3. 4) Defective Interface Board 1A1.

Table 5.5
(continued)

ASSEMBLY	ADJUSTMENTS AND PERFORMANCE
8 "E2" appears in RADIO/BITE Display; other Displays blank.	1) Press "C". If displays return to normal, fault was a momentary loss of 9 volts or 13 volts. 2) If E2 reappears: a. Defective Power Supply 1A22A1. (amber LED's indicate status of 5, 9 and 13 volt regulators). b. Short circuit or excessive load on 9 or 13 volt bus. c. Short circuit on "PS BITE" line on mother board to Logic Board 1A3, pin 13.
9 Frequency continues to change with Tune Knob centered.	1) Defective Interface Board 1A1. 2) Defective or unplugged Display Board Connector 1A21A1P1. 3) Spring retainer loose on Display Board Tune Pot R55. 4) Frequency "CENTER" Pot 1A1R42 on interface board misadjusted.
10 Front Panel Displays and Switch LEDs dim or not lit.	1) Display Board 1A21A1 defective (5 volt DIM circuit). 2) Keypad Board 1A21A2 defective.
11 Inoperative Meter/ Switches.	1) Display Board 1A21A1 defective. 2) Keypad Board 1A21A2 defective.
12 Operation of Displays and Switches not correct.	1) Display Board 1A21A1. 2) Keypad Board 1A21A1. 3) Interface Board 1A1. 4) Logic Board 1A3.
13 No response from Front Panel Switches (check that Remote Switch is in "OUT" position and not lit).	1) Keypad Board 1A21A2. 2) Interface Board 1A3. 3) Logic Board 1A3.

5.7 MOTHER BOARD, 1A1A2

The mother board is a .125 inch PC board 12 1/2 x 16 1/2 inches which serves mainly as a signal interconnection between twenty plug-in PC boards (via 44-pin edge card connectors), a rear panel assembly and a front panel assembly. The board is also used to enforce the mechanical stability of the chassis and to complete the shielding integrity of the metal "card cage" around the signal path and synthesizer boards.

5.7.1 FILTER SWITCH LOGIC

U1 is a NAND gate which produces a 9-volt output (turning on FET switch, Q1) when any of its outputs are low. The inputs are filter-enable signals for the standard IF filter board. This in effect connects the IF signal from IF filter #1 to audio squelch board #1 (via Q1 and C2) when any filter in that board is selected. When no filter is selected, all inputs to U1 are high, U1 output is low and Q1 is off, disconnecting IF filter 1. At the same time an inverted signal from U1 turns Q2 on, connecting IF filter 2 to audio squelch 1. Q3 is a source follower to provide a buffered IF signal monitor output.

5.7.2 AGC CONTROL

Q6 is a low pinch off FET which connects both AGC lines allowing both IF boards to be controlled by audio squelch #1. A TTL low on the ISB line turns Q6 off allowing the AGC of IF filter 2 to be independently controlled by audio squelch board 2.

5.7.3 IF BUFFER AMPLIFIERS

Q4 and Q5 are 5 MHz JFET buffer amplifiers to provide two IF outputs from the mixer board. The input impedance of the two FET's in parallel present a near 50 ohms load to the mixer board output from pin 36. Each FET is tuned and matched at the output (L26, C40, R16 and L27, C41, R17) to present a 50-ohm source impedance to IF filter #1 (pin 36) and IF filter #2 (pin 36) with a net 0 dB gain.

5.7.4 I/O EXPANDERS FOR SYNTHESIZER AND OPTION CONTROL

U2, U3 and U4 are I/O expanders operated from microprocessor outputs from the logic board to control the BCD frequency control inputs of the minor loop, major loop and the BFO board. U4 also has option-enable inputs via jumpers R11 through R14. U2 has two outputs to control a preselector option.

5.7.5 OPTION JUMPER CIRCUITS

Jumpers on the mother board are used to vary the circuit configuration to recognize various options of the radio. JP1 is a 2-pin shorting jumper that directs a LSB signal from the logic board (via the interface board) to pin 37 of IF filter #1 which activates FL2 (the LSB filter in the -001 IF filter board). When a second IF filter is used (as with ISB or IF filter options), the LSB filter is contained in IF filter #2 in the FL1 position and is activated by the LSB signal on pin 34 of J12. JP1 is removed in this configuration to prevent FL2 of IF filter #1 from being activated. The IF filter #2 contains a 100-ohm resistor between pin 38 and 40 which routs the VWIDE signal.

The standard 600-ohm line audio from J10 is normally routed through JP2 and JP3. When the FM option is installed, the jumpers are removed and the audio goes into the FM board

(J6-6, 14) where it is reproduced as balanced outputs (J6-5, 7) with FM audio added to it. T1 and T2 are 600-ohm audio transformers which produce unbalanced signals for meter detection and remote control processing.

JP4 is removed for the BFO option allowing the variable BFO output (J7-37, 38) to be used for the 3rd LO instead of the fixed 5 MHz from the reference board. In the standard radio without BFO, JP6 connects the AM/FM line to the reference board which internally disables the 5 MHz output when either AM or FM detection modes are selected. When BFO is installed, JP6 is removed and JP5 is installed grounding the 5 MHz disable line to the reference board for all detection modes.

R11 through 14 are zero-ohm resistors which ground data inputs to U4. These inputs allow the microprocessor to recognize the options installed and alter the program accordingly. R11 through 14 will be for ISB, FM, Filter, and BFO options respectively. Adding the resistor will enable the option programming.

5.7.6 MOTHER BOARD ACCESS AND REMOVAL

All components except coax wiring are mounted on the top side of the board including option jumpers and integrated circuits (which are mounted in sockets). These may be reached by removing the top cover with 2 quarter-turn fasteners, the top shield with 8 screws and adjacent modules as necessary.

Access to connector pins of all plug-in modules on the bottom of the mother board is accomplished by removing the 8 bottom cover screws.

Removal of the mother board is accomplished by removing the top and bottom cover and top shield as before. Then disconnect the rear panel cable assemblies that connect

to J22, J26, J29, J31 and J36. Also disconnect the power supply cable (P27) to power supply assembly J2. Disconnect ribbon cable assemblies from the front panel to the interface board A1-J1, J2 and J3, and remove all pluggable modules. The mother board is then removeable by 15 screws to the chassis.

MOTHER BOARD
(601212-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1-5,12-18, 27,33-37,39, 42-44	Capacitor, .01µf, 50V	600272-314-002
C38,8-11,19-26,28-32	Capacitor, .10µf, 50V	600272-314-001
C40,41	Capacitor, 200pf	620003-306-501
CR1-7,9-12, 16,17	Diode, 1N4148	600109-410-001
CR18-25,8	Diode, 1N270	600052-410-001
J1-4,6-20,34	Connector, housing	600125-605-001
J1-4,6-20,34	Connector, 22 pin strip	600125-605-002
J22	Header, 26 pin	600174-608-022
J26,29,31	Connector, coax.	600198-606-002
J32,35	Header, 16 pin	600174-608-003
J36	Connector, 3 pin molex	600237-608-002
JP1-6	Connector, mod. 2 pin	600279-608-001
(JP1-6)	Jumper, 2 pin	600190-608-001
L1-7,9-24, 28-30	Choke, 33µH	600125-376-007
L25	Choke, 180µH	600125-376-022
L26,27	Choke, 5.6µH	600125-376-043
P27	Cable assy., 12 pin	600521-540-001
Q1-5	Transistor, J310	600259-413-001
(Q1-6)	Transistor pad,(TO-18)	600025-419-001
Q6	Transistor, 2N3972	600309-413-001
R1,4,5	Resistor, 1KΩ, 1/4W, 5%	610014-341-075
R2,3,6,18	Resistor, 10KΩ, 1/4W, 5%	610024-341-075
R7,20	Resistor, 100KΩ, 1/4W, 5%	610034-341-075
R8	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R9,10	Resistor, 51KΩ, 1/4W, 5%	651024-341-075
R11-14	Resistor, 0Ω, 1/4W, 5%	600000-314-075
R15	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R16,17	Resistor, 680Ω, 1/4W, 5%	668004-341-075
R19	Resistor, 51Ω, 1/4W, 5%	651094-341-075
R21	Resistor, 12KΩ, 1/4W, 5%	612024-341-075
T1,2	Transformer, audio	635234-501-001
U1	IC, 4012B	600178-415-101
U2-4	IC, 8243	600217-415-101
XU1	IC socket	600206-419-014
XU2-XU4	IC socket	600206-419-024
Z1	Resistor network, 1K x 5	600201-537-002

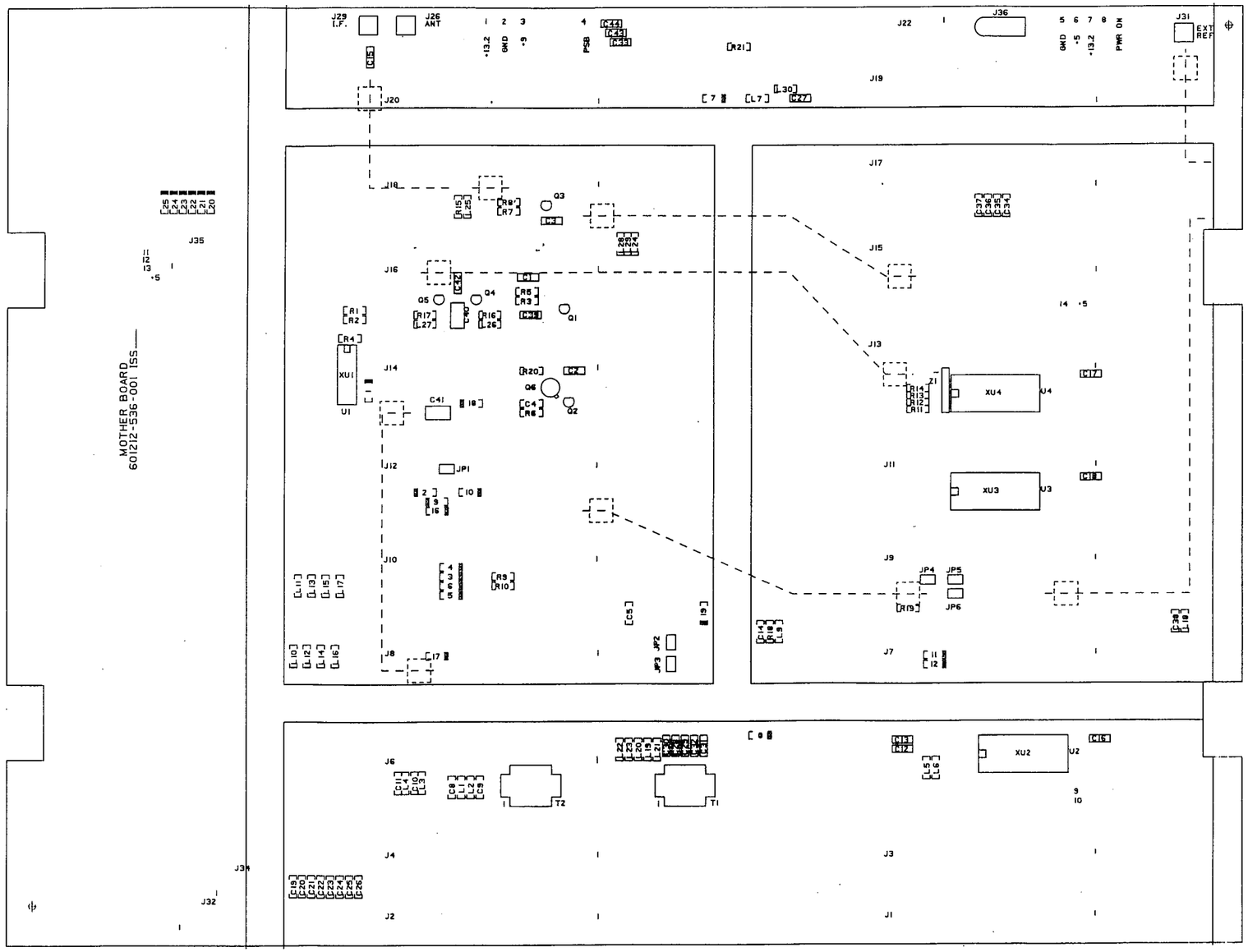
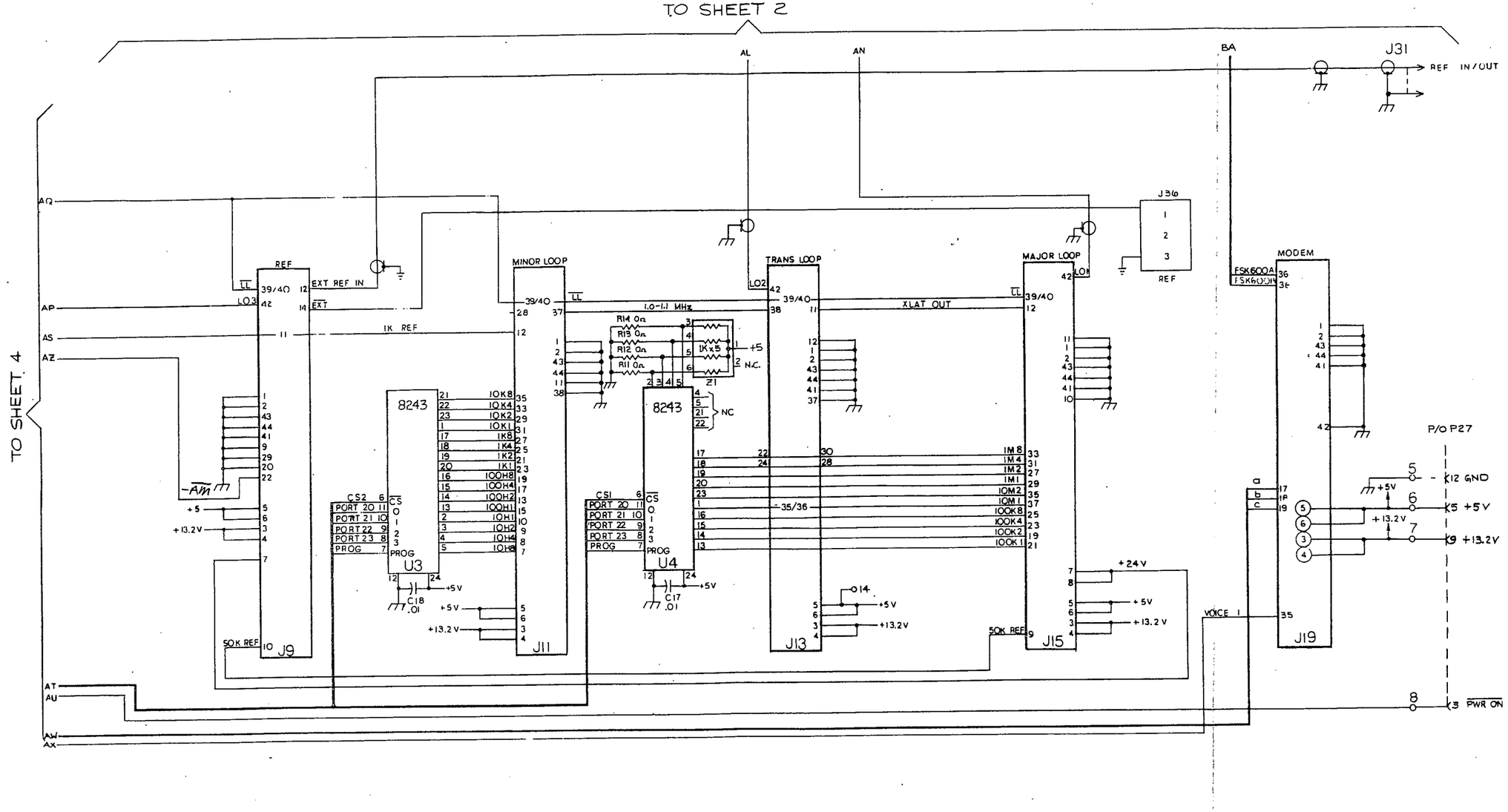


Figure 5.6 Mother Board Assembly



NOTE

1. UNLESS OTHERWISE NOTED:
   ALL RESISTORS ARE IN OHMS, 1/4 WATT, 5%.
   ALL CAPACITORS ARE IN MFD.

   ALL DIODES ARE IN4148

Figure 5.7 Mother Board Schematic
(Sheet 1 of 4)

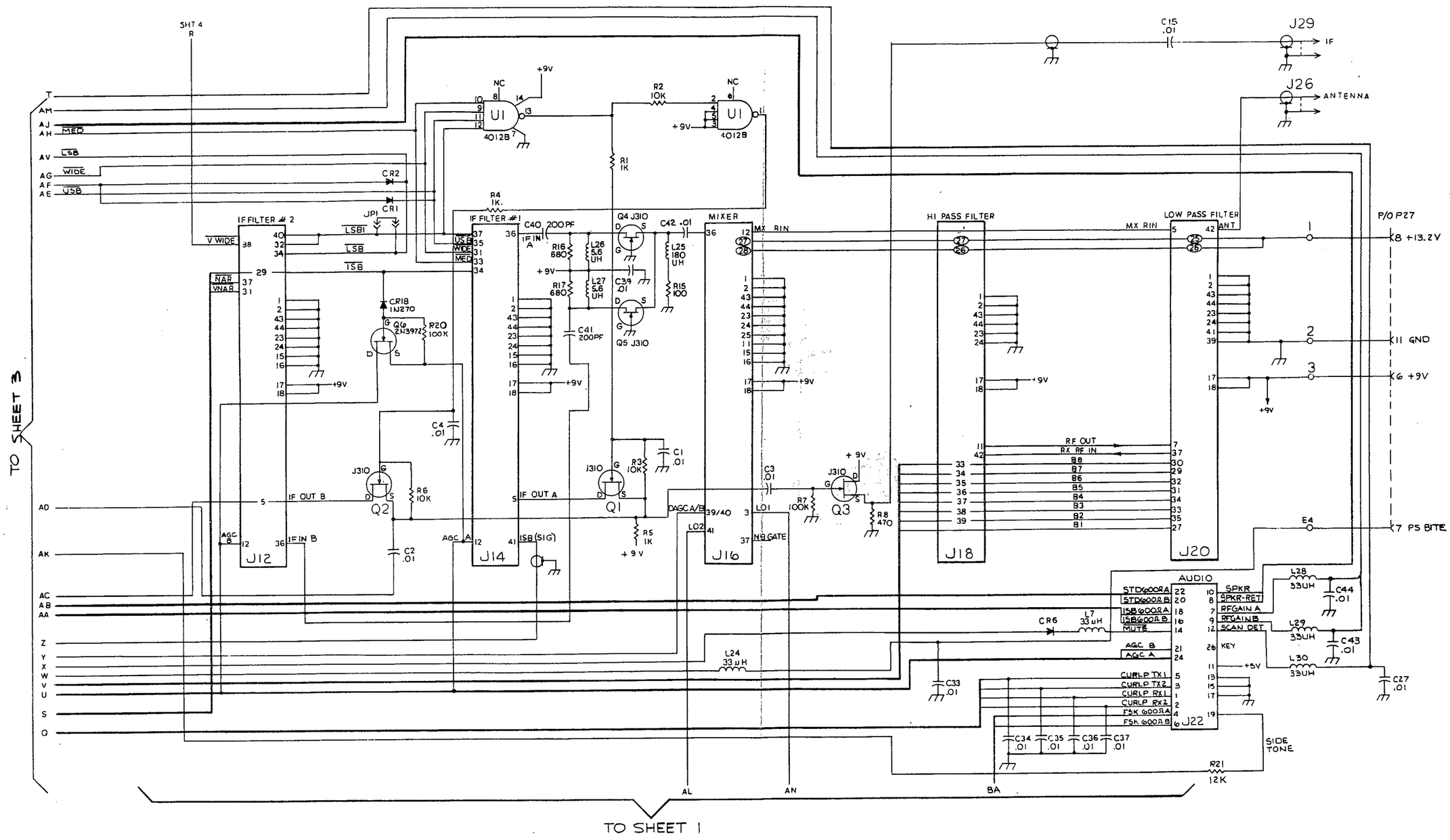


Figure 5.7 Mother Board Schematic
(Sheet 2 of 4)

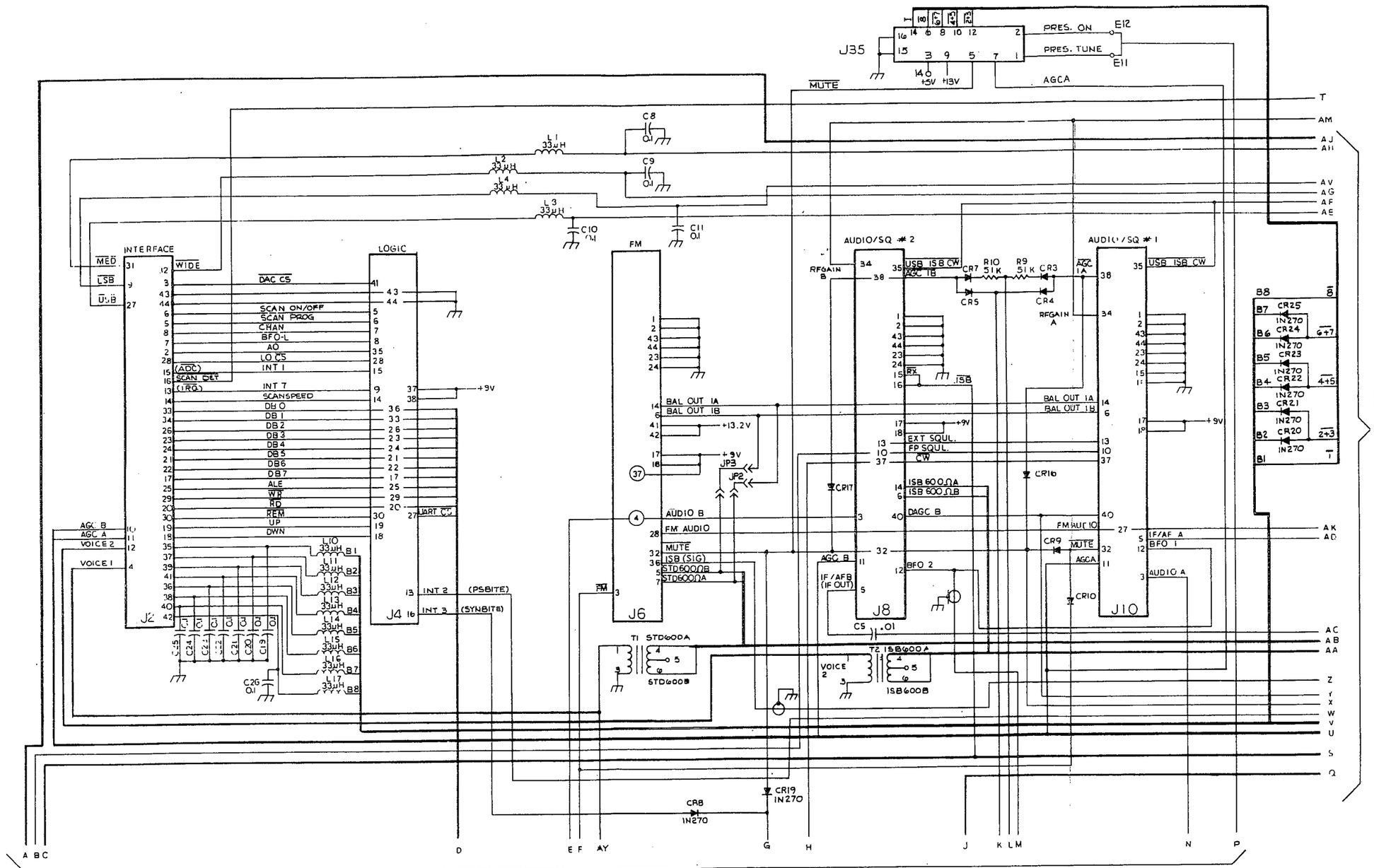


Figure 5.7 Mother Board Schematic (Sheet 3 of 4)

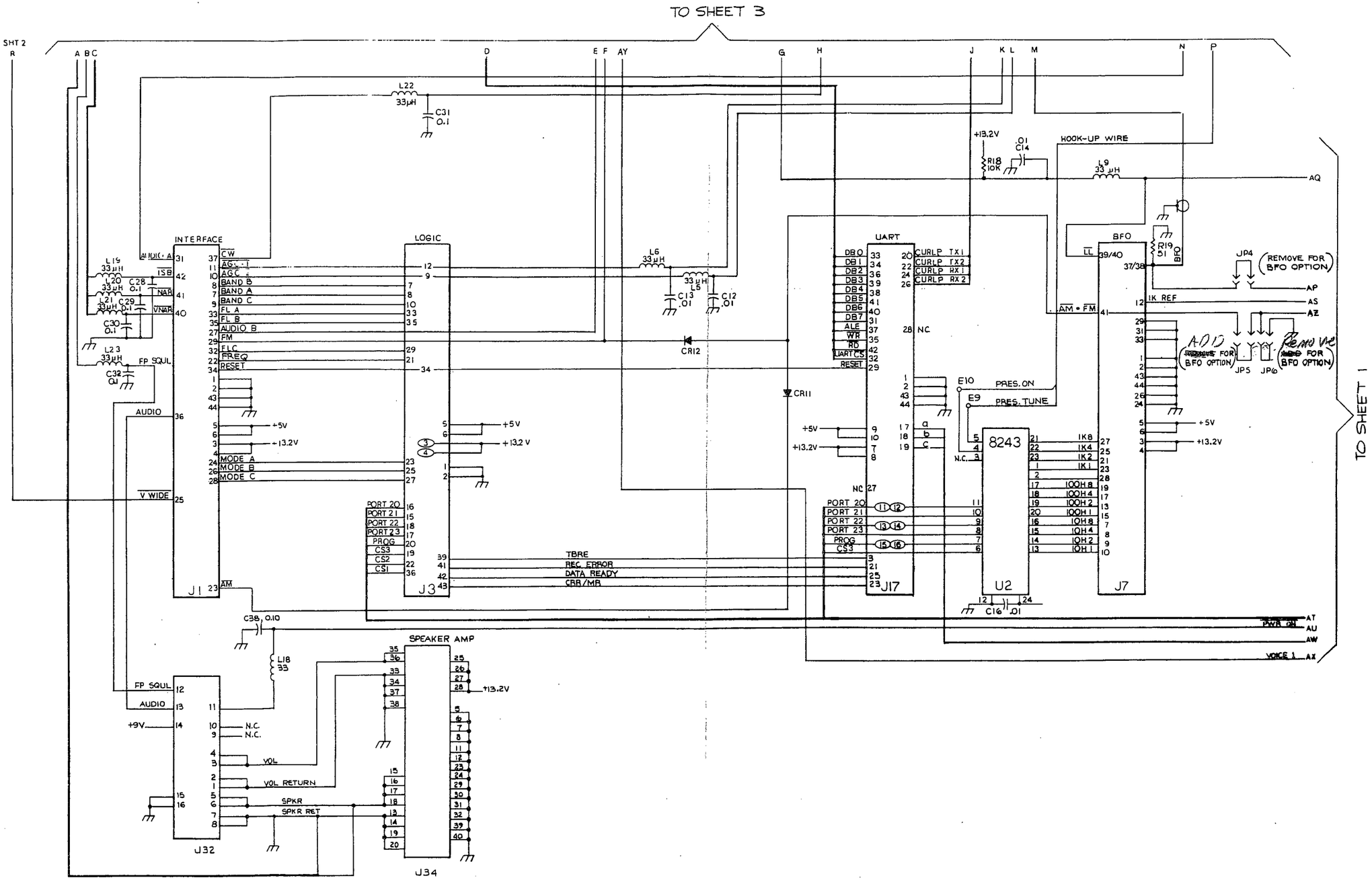


Figure 5.7 Mother Board Schematic
(Sheet 4 of 4)

5.8 INTERFACE BOARD, 1A1A1

The Interface Board is a plug-in PC board with dual 44-pin edge-card connections. It serves mainly as an interconnect between the MSR 5050 two front panel boards and the mother board. Connection is made to the front panel boards via three ribbon cable connectors: J1 (26-pin) to the Display Board, J2 (16-pin) to the Display Board and J3 (34-pin) to the Keypad Board. The Interface Board is also used in the MSR 6406 Remote Control Unit.

5.8.1 KEYBOARD/DISPLAY CHIP

U9 is Keyboard/Display Chip 8279 which is used to perform key scanning and display refreshing. This chip interfaces with the microprocessor through common bus DB0 thru DB7, write command WR, read command RD, and clock signal ALE.

Information from the microprocessor is written into U9 during the write cycle if CS (U9-22) is low during this period. Information obtained is data if A0 is low during write cycle and is command if A0 is high during this period. Scan line SL0 through SL3 (U9-32 through 35 respectively) is a 4-bit encoded signal generated in U9 for key matrix and display scanning. All four bits are used for 16-digit display, but only the three LSB's are used for key matrix scanning.

Return line RL0 through RL7, (U9-38, 39, 1, 2, 5, 6, 7 and 8 respectively) are return signals from the key matrix. These lines are internally pulled up in U9 and can only be pulled low by a key closure.

B0, B1, B2, B3, A0, A1, A2 and A3 form an eight-bit word for the segments of LED display. Note that B0 is LSB.

U9-4 is IRQ output. This pin is normally low and will go high when a key is closed and will go low again after the key code has been read.

U9-9 is reset input. U9 will be reset when this pin goes high.

5.8.2 D-TO-A CONVERTER CHIP

U8 is 8-bit DAC chip to perform A-to-D conversion for the receiver and D-to-A conversion for the remote control unit.

In A-to-D conversion the converter output U12-7 is connected to a comparator U12D to compare with the incoming analog signal. The microprocessor will send out a stepping up digital signal starting from zero. As a result, the voltage in U12-7 will go up accordingly until its value equals the analog signal in U12-12. The comparator output U12-14 will change from high to low at this moment to interrupt the microprocessor chip to stop the stepping up action. The digital signal obtained at this moment is the equivalent digital value of the analog signal and the A-to-D conversion is completed.

In D-to-A conversion the converter output U12-7 is connected to the meter circuit directly to drive the meter.

5.8.3 DECODERS

U1 decodes band information from the Logic Board (Bands A, B and C) and produces TTL low outputs (B1-8) to control the switching of filters in the low pass and high pass filter boards. U2 and U3 operate in parallel to decode filter bandwidth data (FLA, B, C) to produce TTL low outputs to control filter selection in the IF/filter boards (U3, pins 1-6) and to light LED's in the

keypad initiating button (U2, pins 1-6). A decoded 5 (pin 6 of U2 and U3) will be used for FSK with a narrow offset filter in future options. Pin 6 of U3 is bussed to pin 4 to control the VNAR line which corresponds to the physical position on the optional IF/filter board (FL3) where the FSK filter must be placed. Pin 6 of U2 is bussed to pin 3 to light the NAR key LED. U4 and U5 operate similarly to control mode selection lines (U5, pins 1-7) and the corresponding key button LED (U4, pins 1-7). The 74LS145 has open collector outputs to allow pull-ups to 9 volts for control and to 5 volts for LED's. U10C produces a TTL low (via Q1) only when both lines P1-10 and P1-11 are high. U18B and U17 are used as LED drivers.

5.8.4 FREQUENCY SCAN CIRCUITS

A variable rate pulse is generated on either P2-18 or 19 as the DC voltage on J2-4 goes above or below 2.5 VDC. U7 A, B and CR9 and 10 form an absolute value detector which produces an output DC voltage proportional to the difference between 2.5 volts and the input voltage. The output pulls down the base of Q2 via R35 or R33/CR13 to vary the current in Q2. The current in Q2 controls the charge rate of C24 and thus the pulse output frequency of the timer (U13A). U13B acts as a constant pulse width inverter. U7C and D are biased to produce +5 volts output when the input is slightly above 2.5 volts (U7D) or slightly below 2.5 volts (U7C). The outputs are gated through U10A (up control) or U10B (down control) with the slight difference in bias assuring a dead zone where neither U10A nor B are gated on.

5.8.5 METER CIRCUITS

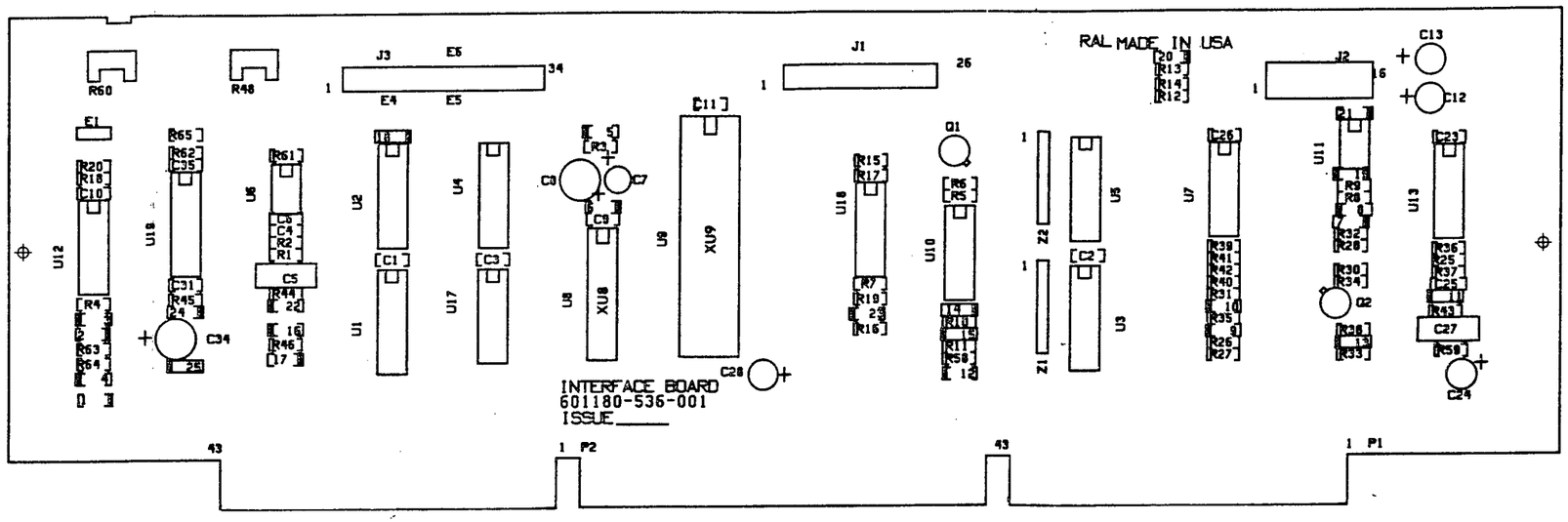
Audio inputs on P1-4 and 12 are rectified (CR7 and CR8) and peak detected (U11A, B and CR19, 21) to produce DC outputs proportional to audio level to drive a meter.

5.8.6 CHANNEL SCAN CIRCUITS

The Scan Circuitry is enabled by a TTL high on P2-6 which allows the scan oscillator U12A to start (by grounding C28 via U18A) and arms the scan delay monostable U19A by removing the TTL low on the clear input, pin 3. U12A oscillates at a rate determined by C28 and a 100K variable resistor on the keypad board accessable from the front panel. The output is differentiated and limited to 5 volts peak to drive the logic board microprocessor (via P2-14). The microprocessor will iniate a channel change upon receiving the scan oscillator pulse unless a TTL high is produced from the scan delay monostable U19A-6 (via P2-18). If a high is sensed, the microprocessor will change channels as soon as the scan delay output goes low. When the channel changes, a narrow TTL low pulse ($\approx$ 2 Msec) is put on P2-6 which triggers a signal inhibit one-shot U19-B (pin 11) producing a 100 Msec (C35, R62) TTL high pulse (pin 10). This raises the trigger threshold (set by R48) on signal detector U12C (pin 10), thus prohibiting triggering on transient signals during channel change.

Audio signals coming into comparator U12C-9 above a threshold voltage (set by R48) will produce negative-going pulses to trigger the scan delay monostable, U19 (pin 4). The scan delay is variable by R60 in conjunction with C34 from .5 to 5 seconds. When U19A is triggered a

TTL low signal is put out from U19-7 (Q) to P2-16 to indicate signal presence. With jumper JP2 between E2-2 and 3, U19 cannot be retriggered during the scan delay period. At the end of the delay period, the rising pulse from Q (U19-7) triggers the signal inhibit monostable at U19-12 to prevent retrigger until the channel is changed. The same rising edge of Q triggers the scan oscillator via C36 to ensure that the scan dwell for the next channel will be a full period.



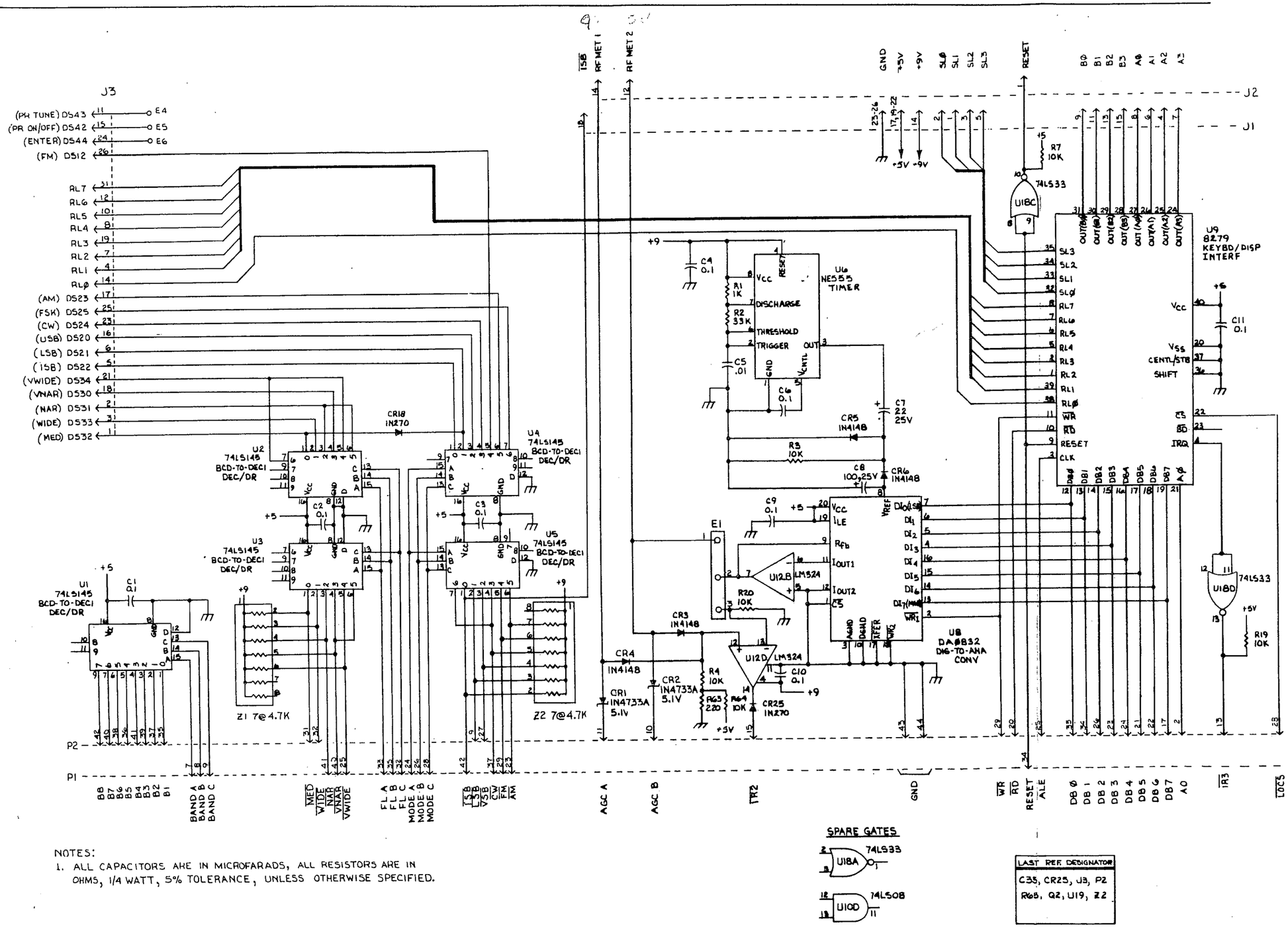
INTERFACE BOARD
(601180-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1-4,6,9-11,23, 26,31,35	Capacitor, 1µf., Cer.	600272-314-001
C7	Capacitor, 22µf, 25V	600297-314-016
C8,34	Capacitor, 100µf, 25V	600297-314-032
C12,13,28	Capacitor, 10µf, 25V	600202-314-018
C24	Capacitor, .33µf, 35V	600202-314-004
C25	Capacitor, .001µf, Cer.	600272-314-008
C25,27	Capacitor, .01µf, Mylar	600204-314-001
CR1,2	Zener, 5.1V, IN4733A	600006-411-006
CR3-10,16,17,19 -24, CR11,14,15, 18,25	Diode, 1N4148 Diode, 1N270	600109-410-001 600052-410-001
CR12	Zener, 9.1V, 1N4739A	600006-411-012
CR13	Zener, 3.3V, 1N746A	600002-411-001
E1	Header, 3 pin	600198-608-005
J1	Connector, 26 pin	600174-608-005
J2	Connector, 16 pin	600174-608-003
J3	Connector, 34 pin	600174-608-006
Q1	Transistor, 2N2222A	600080-413-001
Q2	Transistor, 2N2907A	600154-413-001
R1,18,45,59	Resistor, 1K, 1/4W, 5%	610014-341-075
R2,35	Resistor, 33K, 1/4W, 5%	633024-341-075
R3,4,7-15,17,19, 20,43,44,62,32,64	Resistor, 10K, 1/4W, 5%	610024-341-075
R5,33,34	Resistor, 4.7K, 1/4W, 5%	647014-341-075
R6,61	Resistor, 2.2K, 1/4W, 5%	622014-341-075
R16	Resistor, 20K, 1/4W, 5%	620024-341-075

INTERFACE BOARD
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
R25	Resistor, 3.3M, 1/4W, 5%	633044-341-075
R26	Resistor, 180K, 1/4W, 5%	618034-341-075
R27,46	Resistor, 100K, 1/4W, 5%	610034-341-075
R28	Resistor, 5.6K, 1/4W, 5%	656014-341-075
R29	Resistor, 1.5K, 1/4W, 5%	615014-341-075
R30	Resistor, 150K, 1/4W, 5%	615034-341-075
R31	Resistor, 120K, 1/4W, 5%	612034-341-075
R36,63	Resistor, 220K, 1/4W, 5%	622004-341-075
R37,65	Resistor, 47K, 1/4W, 5%	647024-341-075
R38	Resistor, 51K, 1/4W, 5%	651094-341-075
R39,42	Resistor, 5.11K, 1/8W, 1%	651111-342-059
R40,41	Resistor, 6.19K, 1/8W, 1%	661911-342-059
R48	Resistor, VAR, 10K	600089-360-010
R58	Resistor, 200K, 1/4W, 5%	620004-341-075
R60	Resistor, VAR, 100K	600089-360-014
U1,2,3,4,5	IC, 74LS145	600528-415-001
U6	IC, NE555	600074-415-001
U7,12	IC, LM324	600171-415-001
U8	IC, DAC0832	600605-415-001
U9	IC, 8279	600507-415-101
U10	IC, 74LS08	600271-415-001
U11	IC, LM358	600150-415-001
U13	IC, NE556	600237-415-001
U17,18	IC, 74LS33	600219-415-001
U19	IC, 4528B	600191-415-101
	Transistor pad	600025-419-001
XU8	Socket, IC-20 pin	600119-419-020
XU9	Socket, IC-40 pin	600119-419-040
Z1,Z2	Resistor Net. 7 @ 4.7K	600201-537-001

Figure 5.8 Interface Board Assembly



NOTES:
1. ALL CAPACITORS ARE IN MICROFARADS, ALL RESISTORS ARE IN OHMS, 1/4 WATT, 5% TOLERANCE, UNLESS OTHERWISE SPECIFIED.

SPARE GATES

LAST REF DESIGNATOR
C35, CR25, J3, P2
R65, Q2, U19, Z2

Figure 5.9 Interface Board Schematic (Sheet 1 of 2)

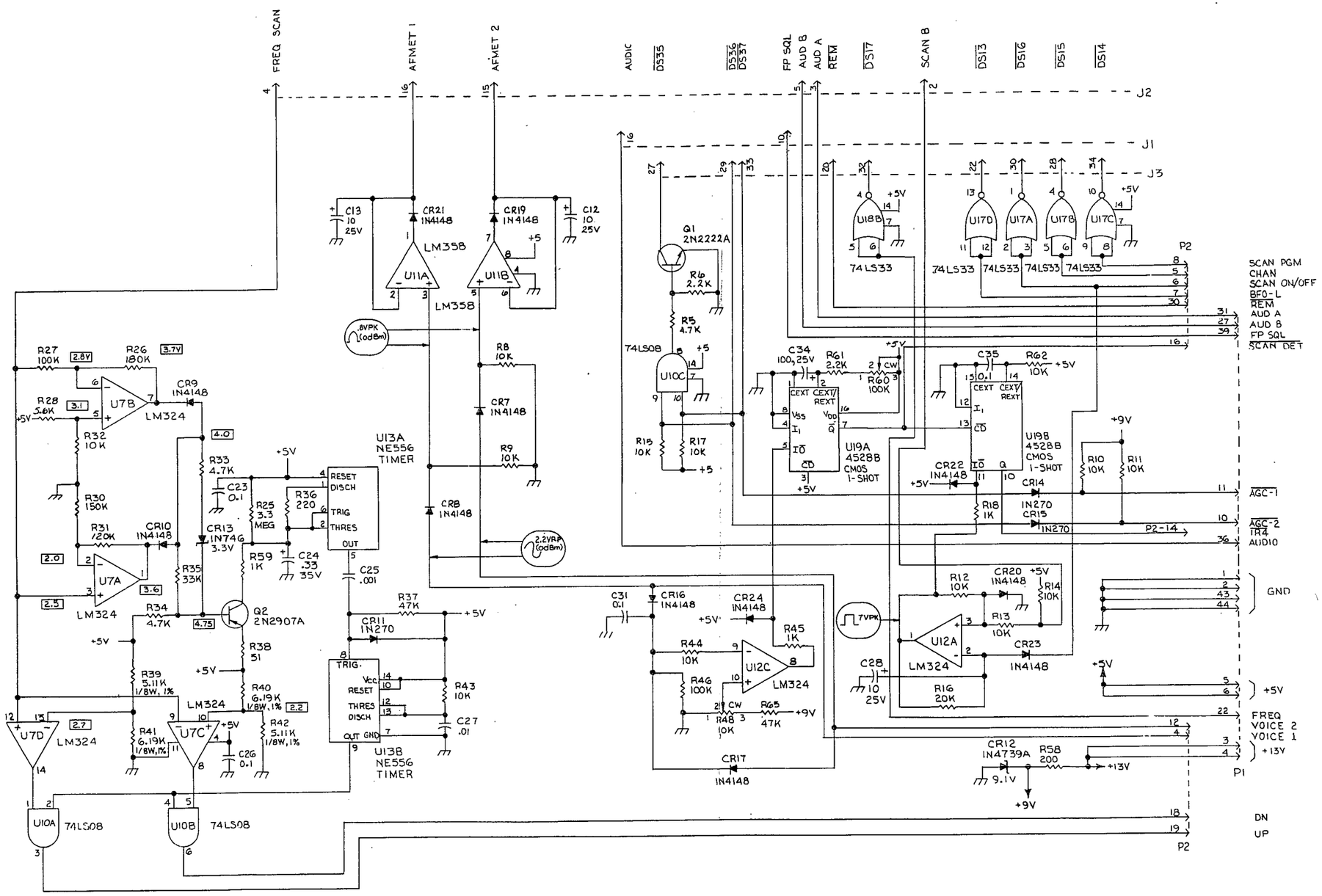


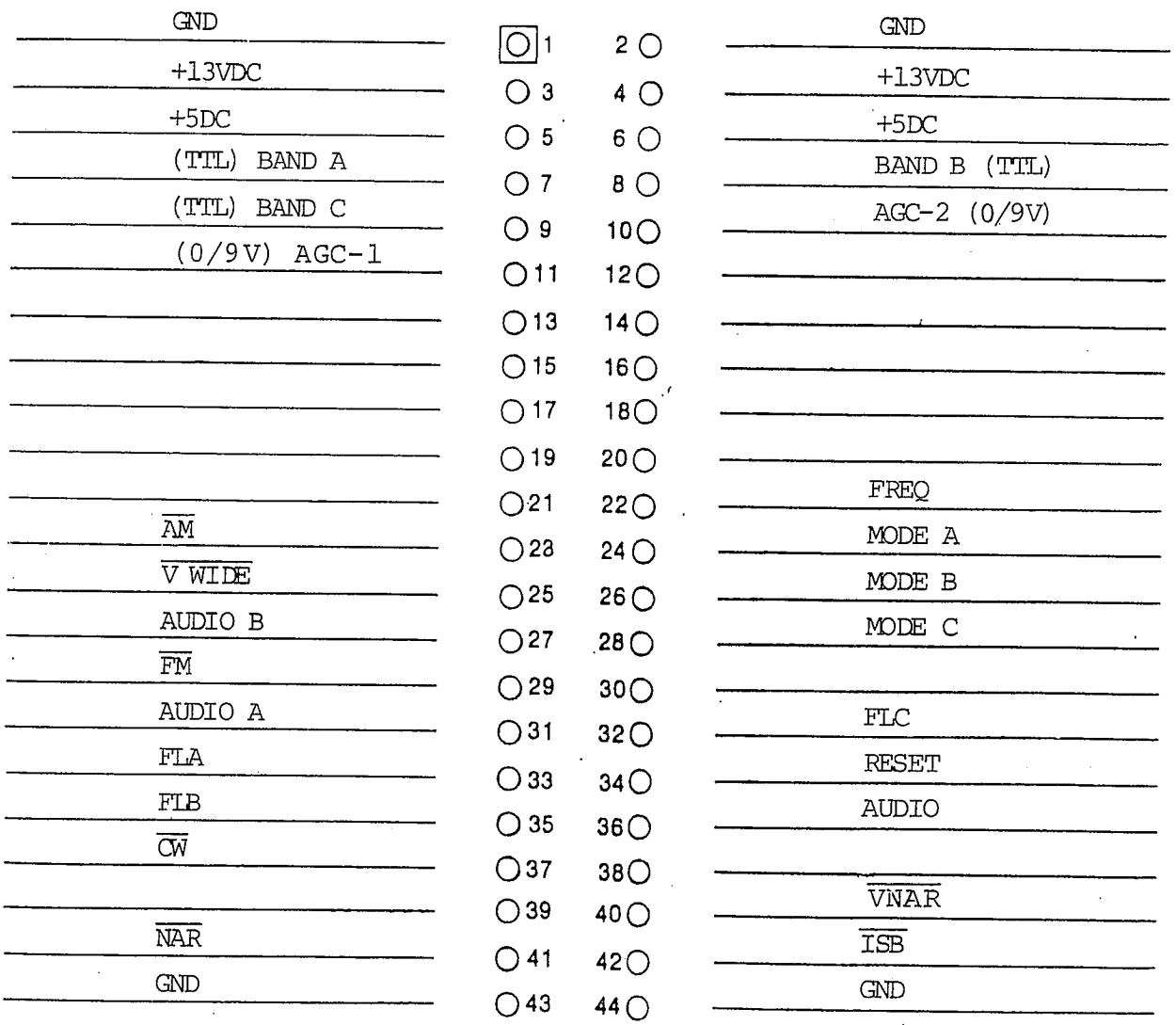
Figure 5.9 Interface Board Schematic
(Sheet 2 of 2)

INTERFACE BOARD

1A1A1

PIN CONNECTIONS/VOLTAGE READINGS

1A1A1-J1



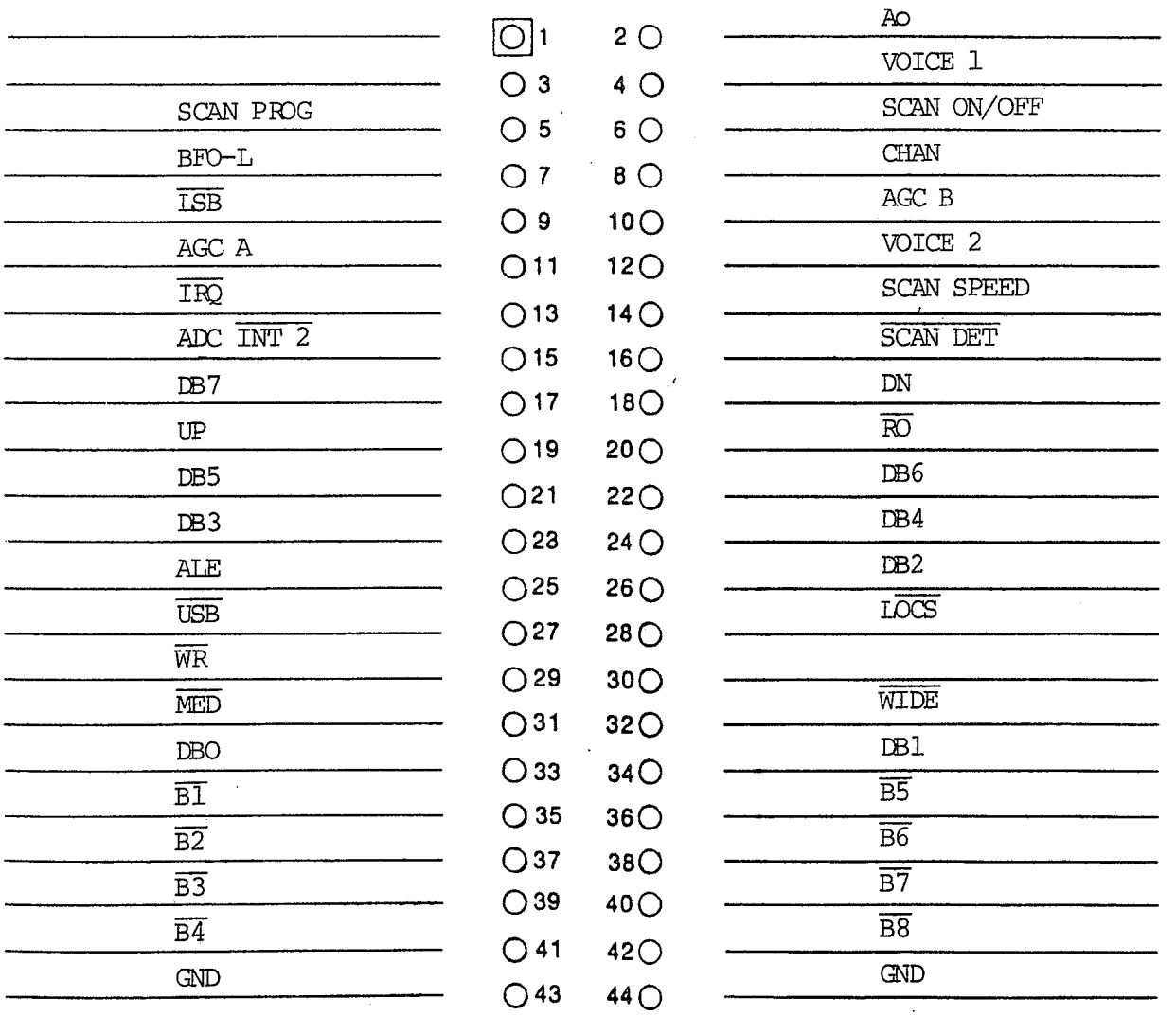
BOTTOM VIEW

INTERFACE BOARD

1A1A1

PIN CONNECTIONS/VOLTAGE READINGS

1A1A1-J2



BOTTOM VIEW

5.9 LOGIC BOARD, 1A1A3

This PC board contains all necessary hardware for software controlling of the whole system. It includes the μP Chip, 8035 (U1); 8 Bit Address Latch, 74LS273 (U3); 2K x 8 Program Memory Chips, 2716 (U4, U15); 1K x 4 Data RAMs, NM6514 (U16, U17); Interrupt Priority Chip, 8214 (U2); I/O Chip Select Decoder, 74LS138 (U10); Memory Chip Select Decoder, 74LS138 (U9); I/O Expander, 8243 (U6, U8); 8 Bit Tristate Buffer, 74LS241 (U11); some supporting logic gates, diodes and transistors.

5.9.1 MICROPROCESSOR CHIP

U1 is 8 Bit μP Chip, 8035, with 4K bite of external program memory and 2K x 4 bits of data RAM for channel data storage. Internal clock frequency is controlled by L3, C19 and C20. Input pins T0 and T1 (pins 1 and 39 respectively) are used for frequency up and down control. Frequency will step up one step (+10 Hz), when T0 is detected by the μP as a logic "1"; and step down one step (-10 Hz) when T1 is detected as logic "1". INT pin (pin 6) interfaces with outside world through priority interrupt chip U2 (8214) to handle more than one interrupt source. Pins 21 thru 25 are used to control 5 I/O Expander Chips (8243) in the system.

I/O chip select signal is generated in output port P24, P25 and P26 (pins 35, 36 and 37) of U1 and decoded by 3 to 8-Line Decoder, 74LS138 (U10) to select one of 5 I/O Expanders in the system. Output port P10, P11 and P12 (pins 27, 28 and 29) is used to output encoded memory chips in the system. Note that in addition to static RAM, MN6514, (U16 and U17); U2 (8214) in Logic Board; the UART Chip, 6402, in UART Board; and the Keypad/Display Chip, 8279, in Interface Board are also considered as memory chips. Memory chip select command is decoded by 3 to 8 Decoder, 74LS138, (U9).

5.9.2 PROGRAM MEMORY CHIP

U4 and U15 are 2K x 8 EPROM 2716 used as program memory chip for the system control program storage. Selection of these chips is controlled by software. U1 P23 (pin 24) goes low when SEL MB0 instruction is given. As a result, U4 is selected. If instruction SEL MB1 is given, U1 P23 will be high to force U5-8 to go low to select U15.

5.9.3 CHANNEL DATA MEMORY CHIP

U16 and U17 are 1K x 4-bit static RAM used for channel data and radio status information storage. Data stored in these chips are 4-bit words. Radio status is stored in U16 memory locations 00H to 1FH. It includes channel number and radio number (two words each) and channel scan information for six blocks of channels. Each block specified the start channel number and the stop channel number (total four words for each block).

Channel data is stored in U16 memory locations, 020H thru 3FFH and U17 000H thru 240H. Each channel occupies fifteen memory locations to store fifteen 4-bit words for each channel including seven words for channel frequency, one word each for BAND, AGC, MODE and FILTER information, and four words for BFO sign and frequency. Memory locations 250H thru 25EH are used for scratch pad channel storage.

5.9.4 I/O EXPANDER

U6 and U8 are I/O Expander Chip 8243. Each chip contains four 4-bit ports that could be used as input or output ports. U8 P5 is output port

for MODE command. U8 P6 is output port for BAND command. U8 P5 is output port for filter select command. U8 P4 is output port for AGC. U6 P4 and P7 provides signal to turn on LED on the function keys when they are depressed. U6 P5 and P6 are for UART controlling.

5.9.5 PRIORITY INTERRUPT CHIP

U2 is priority Interrupt Chip 8214. Eight interrupts can be connected to this chip with assigned priority level. An interrupt output will be generated when the right level of interrupting signal is received. Interrupt level is controlled by software. U14 is connected as FF to store the narrow INT output signal generated by U2. The highest priority input is connected to R7, pin U2-22 and lowest to R0, pin U2-15..

5.9.6 OR GATE U13

OR gate output pin U13-8 will go low during µP read cycle ($\overline{RD}$ low) if U2 is selected (U9-12 low). This signal enables the µP to read the priority level of the interrupt.

U13 output pin U13-11 will go low during µP write cycle ($\overline{WR}$ low) if U2 is selected. This signal enables the µP to set a priority level. Note that only interrupt with priority higher than this set level will be accepted.

OR Gate Output U13-3 will go low during µP read or write cycle if U9-15 is low (keypad chip or UART selected). If local/remote switch is in local position, U13-4 is low. Therefore, U13-6 is low to select Keypad Chip (LO $\overline{CS}$ low). If switch is in remote position, U13-4 will be high and U13-6 high to force U5-2 low. As a result, UART will be selected to obtain control from remote control unit.

5.9.7 OR GATE U12

U12-1 and 13 goes low during µP read and write. If U9-14 is low (U16 selected), then U12-3 is low to force U12-6 low when the clock signal ALE goes low to enable static RAM U16. If U9-13 is low (U17 selected), then U12-11 is also low during read and write cycle to select static RAM U17 when ALE goes low.

5.9.8 POWER OFF PROTECTION

Q1 is biased on in-normal operation. During power turn off, voltage on Q1-E will decrease very fast; yet, the voltage in Q1-B decreases very slowly due to slow discharge of C24. As a result, Q1 will be cut off very quickly to single step U1. This will prevent garbage from being written into data RAM during power turn off.

Q2 is biased off during normal operation. When power is turned off, voltage on Q2-B drops very quickly to turn Q2 on. Therefore, U1-4 goes low to reset the µP during power off to avoid the possible write cycle during this period.

5.9.9 BATTERY SWITCH

Battery BT1 is used to retain data in static RAM U16 and U17 when power is removed from this board. During normal operation, Q3 is biased on to supply +5V to U16 and U17. Under this condition diode CR3 is reverse biased; therefore, battery current will not flow to the RAM.

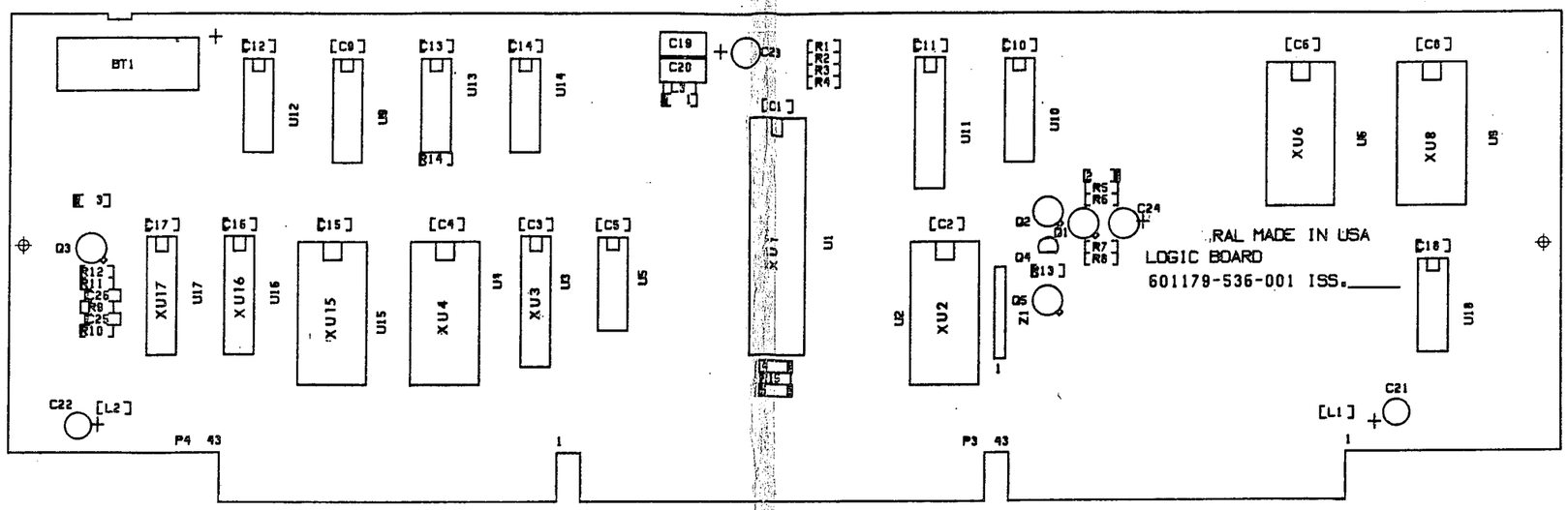


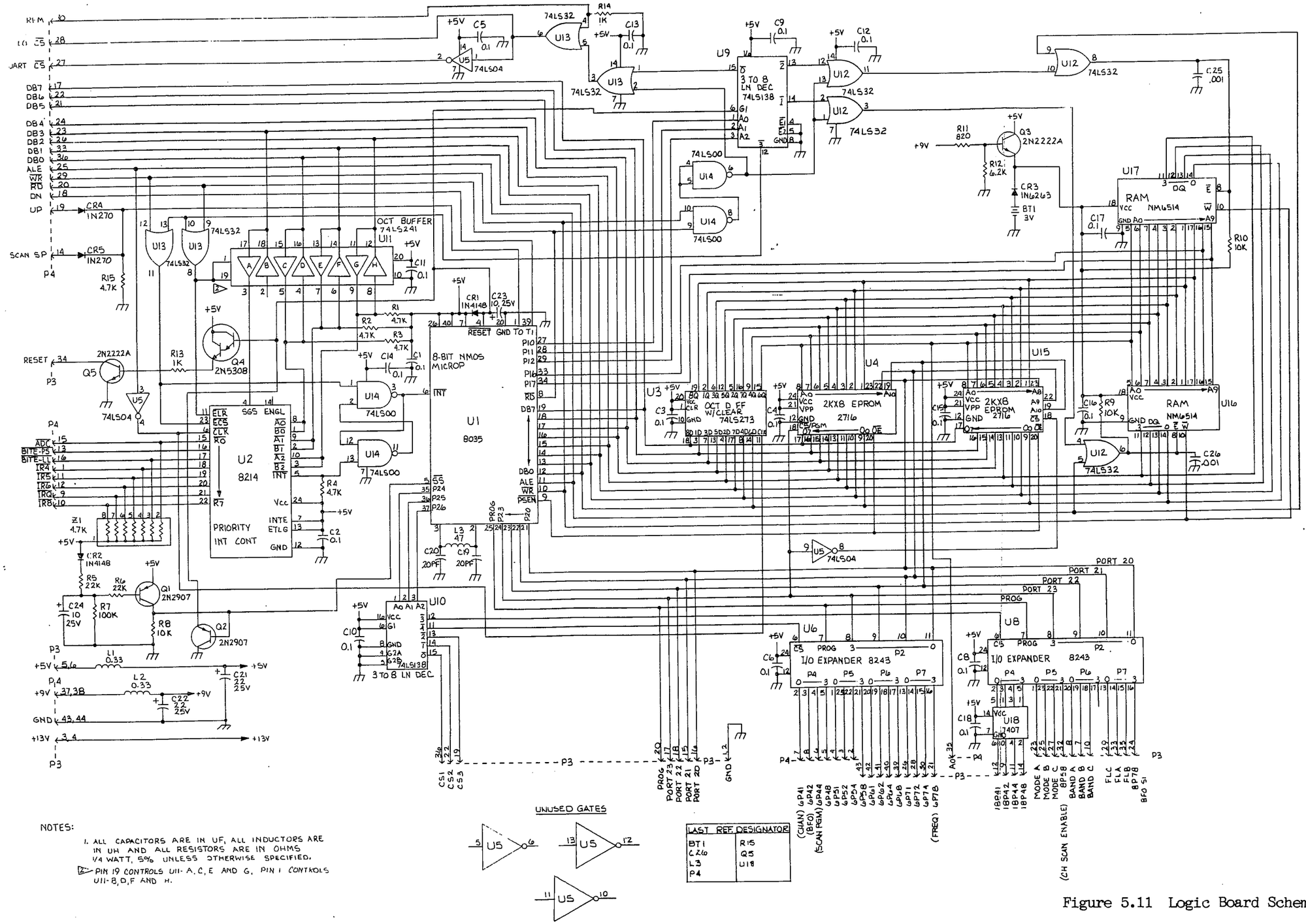
Figure 5.10 Logic Board Assembly

LOGIC BOARD
(601179-536)

SYMBOL	DESCRIPTION	PART NUMBER
BT1	Lithium battery	600027-392-001
C1-6,8-18	Capacitor, 0.1µf, 50V	600272-314-001
C19,20	Capacitor, 20pf, mica	620094-306-501
C21,22	Capacitor, .22µf, 25V	600297-314-016
C23,24	Capacitor, 10µf, 25V	600202-314-018
C25,26	Capacitor, .001µf, 50V	600272-314-004
CR1,2	Diode, 1N4148	600109-410-001
CR3	Diode, 1N6263	600145-410-001
CR4,5	Diode, 1N270	600052-410-001
L1,2	Choke, .33µH	600125-376-001
L3	Choke, 47µH	600125-376-008
Q1,2	Transistor, 2N2907	600154-413-001
(Q1,2,3,5)	Transistor pad (TO-18)	600025-419-001
	TY-wrap	600002-116-002
Q3,5	Transistor, 2N2222	600080-413-001
Q4	Transistor, 2N5308	600221-413-002
R1-4,15	Resistor, 4.7K, 1/4W, 5%	647014-341-075
R5,6	Resistor, 22K, 1/4W, 5%	622024-341-075
R7	Resistor, 100K, 1/4W, 5%	610034-341-075

LOGIC BOARD
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
R8-10	Resistor, 10K, 1/4W, 5%	610024-341-075
R11	Resistor, 820Ω, 1/4W, 5%	682004-341-075
R12	Resistor, 6.2K, 1/4W, 5%	662014-341-075
R13,14	Resistor, 1.0K, 1/4W, 5%	610014-341-075
U1	IC, 8035µp	600218-415-102
U2	IC, 8214	600519-415-001
U3	IC, 74LS273	600277-415-001
U4,15	IC, 2716, 2K x 8	600451-415-101
U5	IC, 74LS04	600111-415-001
U6,8	IC, 8243	600217-415-101
U9,10	IC, 74LS138	600309-415-001
U11	IC, 74LS241	600311-415-001
U12,13	IC, 74LS32	600411-415-001
U14	IC, 74LS00	600114-415-001
U16,17	IC, NM6514	600603-415-001
U18	IC, 7407	600076-415-001
XU1	40 pin IC socket	600119-419-040
XU2,4,6	24 pin IC socket	600119-419-024
8,15		
XU6	20 pin IC socket	600119-419-020
XU16,17	18 pin IC socket	600119-419-022
Z1	Resistor pak, 7 x 4.7K	600201-537-001



NOTES:

1. ALL CAPACITORS ARE IN UF, ALL INDUCTORS ARE IN UH AND ALL RESISTORS ARE IN OHMS 1/4 WATT, 5% UNLESS OTHERWISE SPECIFIED.
2. PIN 19 CONTROLS U11-A, C, E AND G, PIN 1 CONTROLS U11-B, D, F AND H.

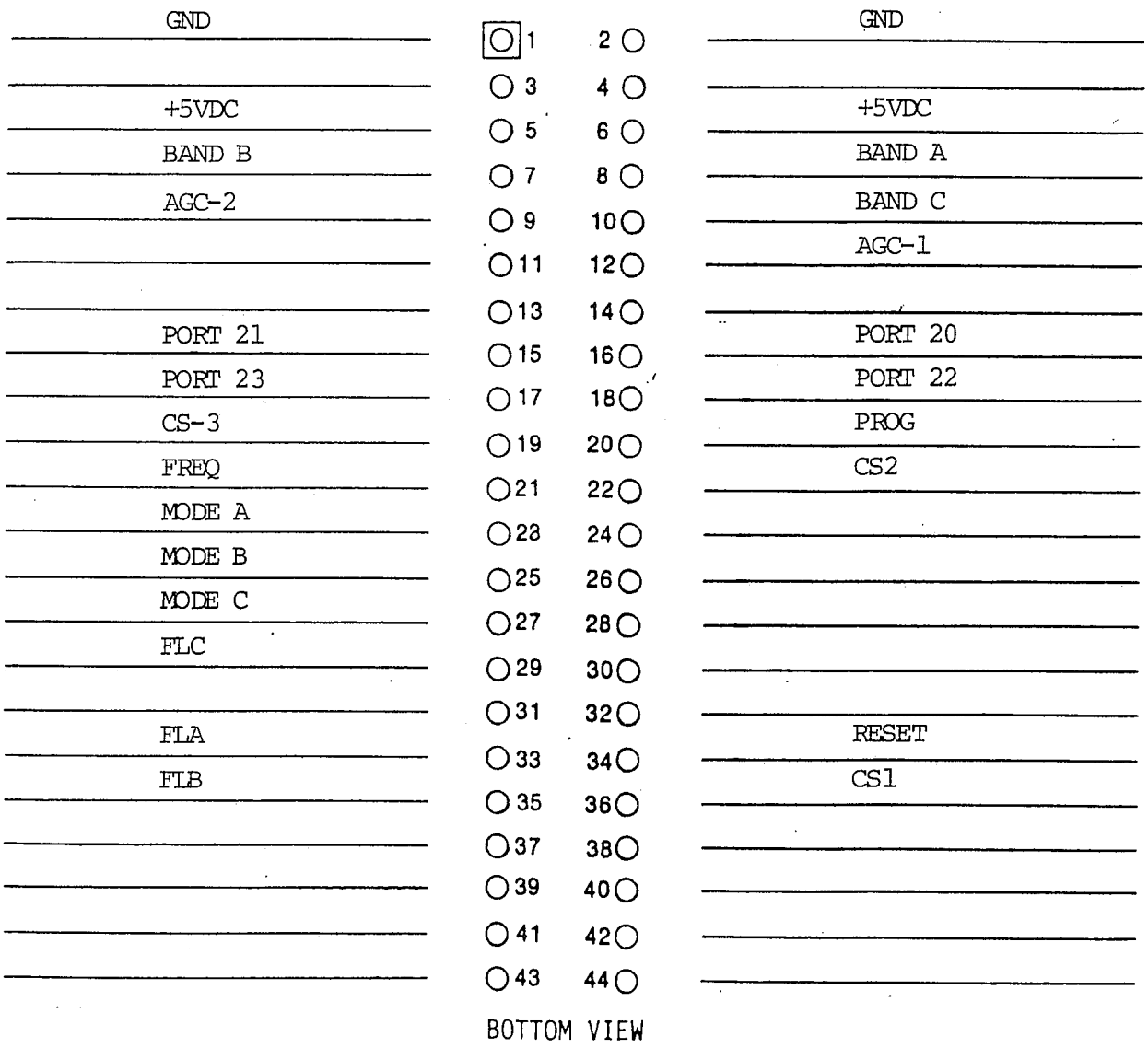
Figure 5.11 Logic Board Schematic

LOGIC BOARD

1A1A3

PIN CONNECTIONS/VOLTAGE READINGS

1A1A3-J3



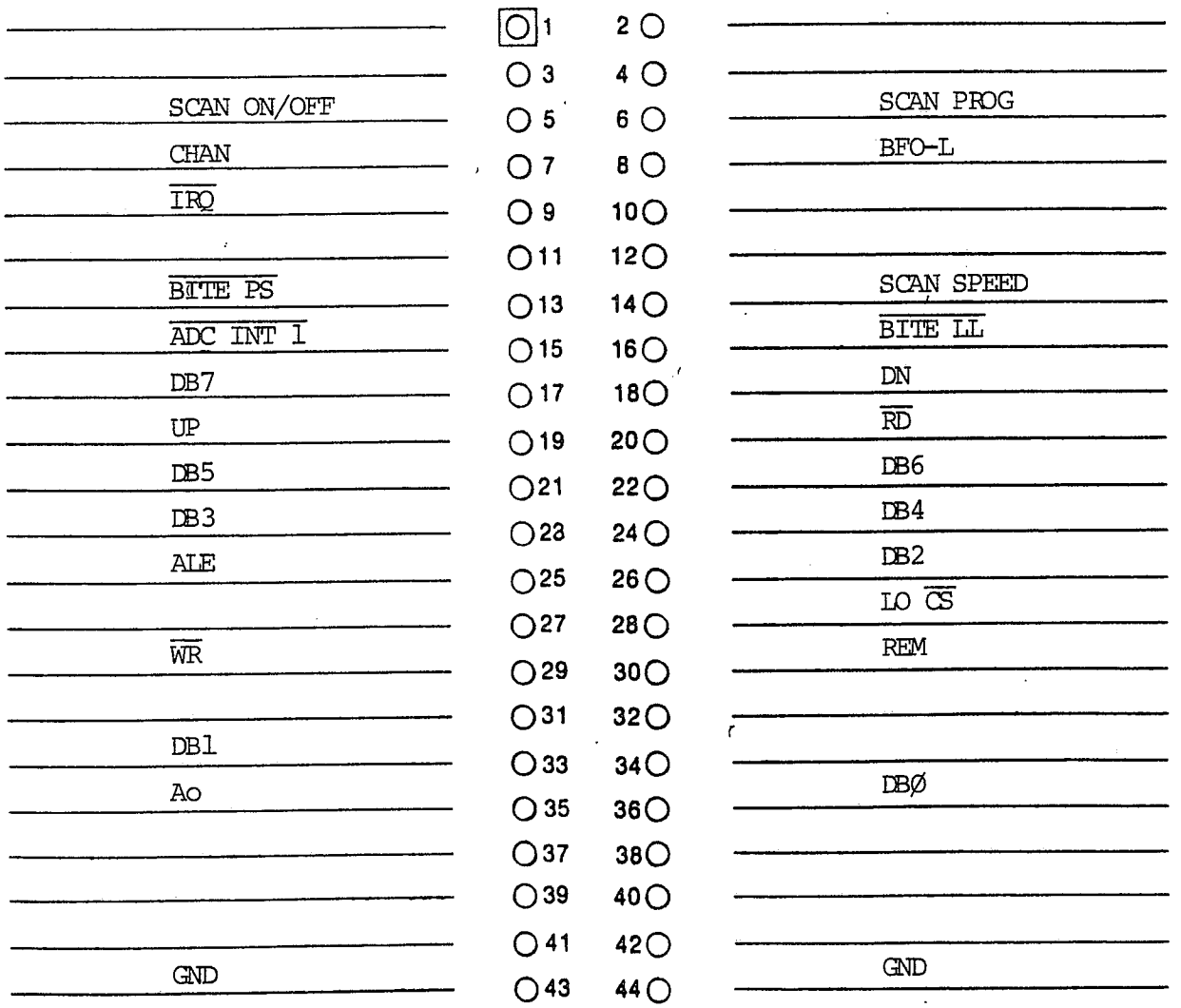
BOTTOM VIEW

LOGIC BOARD

1A1A3

PIN CONNECTIONS/VOLTAGE READINGS

1A1A3-J4



BOTTOM VIEW

5.10 LOW PASS FILTER BOARD, 1A1A20

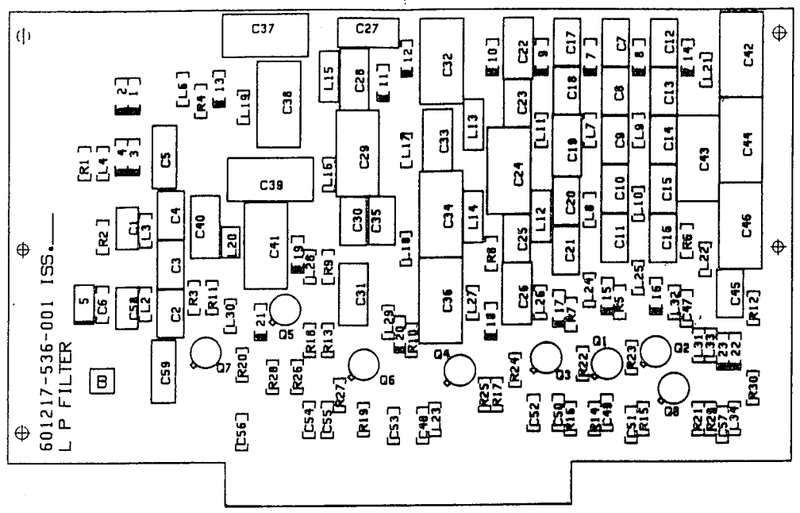
5.10.1 GENERAL

The LP Filter Board contains in series: a 10-watt input protection circuit, a 30 MHz low pass filter and a parallel bank of 8 selectable low pass filters with cutoff frequencies of 2, 3, 4, 6, 9, 13, 20 and 30 MHz corresponding to bands 1 through 8 respectively. The LP filter is normally cascaded with a high pass filter with complementing cutoff frequencies to produce a selectable band pass response in bands 2 through 8. The output of the LP filter (pin 37) feeds the HP filter whose output is returned to the LP filter on pin 7. The cascaded output then is routed to the mixer through CR23 which is always on as long as any band from 2 to 8 is selected. To allow response down to 10 kHz, the HP filter is bypassed in band 1 by connecting the output of the 2 MHz LP filter directly to the mixer board (pin 5) via CR22 with the HP filter isolated by CR23, being off. Each filter is a 7-element, elliptic, low pass design with a 35 dB design stop band. Insertion loss, designed for 0.1 dB at the cutoff frequency, is allowed 2 dB for component Q and Manufacturing tolerances.

5.10.2 DETAILED CIRCUIT DESCRIPTION

Band 8 is switched by pin diodes CR7 and CR15. When a logic 0 is applied to pin 30, Q1 is saturated and 9 volts appears on Q1 collector causing current flow through L24, L7, L8, CR7, CR15, R4, L6, L32, L33, CR23, R30 and L34. The voltage developed across R4 back-biases CR8 through CR14 in the other filters. The voltage across R30 back-biases CR16 through CR22 in the other filters. The selection of bands 2 through 7 are similar with the selected filter output going to pin 37 to a high pass filter board whose output is brought back to the low pass filter on pin 7. Forward-biased CR23 conducts the signal to the combined filter output on pin 5. L32 and L33 isolate the RF signal at pin 5 from that at pin 7. When band 1 is selected by a ground at pin 27, CR22 is biased on, connecting the band 1 filter output directly to pin 5. The resulting voltage drop across R30 isolates the high pass filter signal at pin 7 by the reverse bias on CR23.

The RF input to the board on pin 42 goes through a 7-element, 35 MHz low pass elliptic filter (C2, L3, C1-4 and C58) to reach the bank of 8 filters via C5. A voltage protection cirucuit at C5 consisting of pin diodes CR1-4 and associated bias circuit clip input waveforms above a peak-to-peak level of 6.8 volts. The series combination of CR3/CR4 and CR1/CR2 is back-biased 5.6V by the zener voltage of CR5 with the center point at 2.8V by the divider action of R1 and R2. The negative peaks of the input signal are clamped to ground by CR1/CR2. The positive peaks above 5.6V (plus two diode drops) cause CR3/CR4 to conduct through the near-RF-short of C6 and C49 with residual rectified current dissipated by CR5. The output is then limited to a nominal +20 dBm.



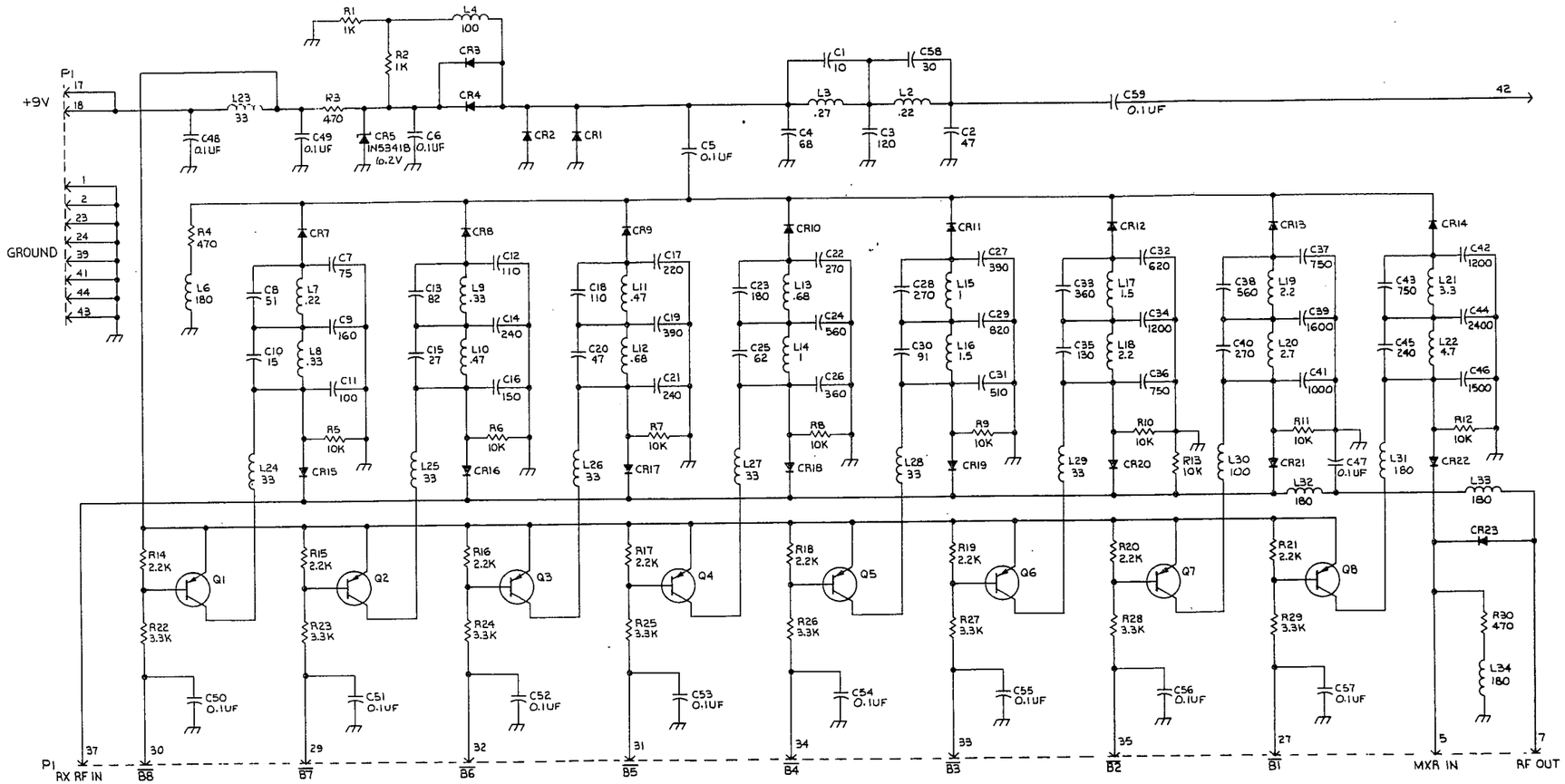
LOW PASS FILTER
(601217-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1	Capacitor, 10pf	610093-306-501
C2,20	Capacitor, 47pf	647093-306-501
C3	Capacitor, 120pf	612003-306-501
C4	Capacitor, 68pf	668093-306-501
C5,59	Capacitor, .1mf, 100V	600204-314-020
C6,47-57	Capacitor, .1mf, 50V	600272-314-001
C7	Capacitor, 75pf	675093-306-501
C8	Capacitor, 51pf	651093-306-501
C9	Capacitor, 160pf	616003-306-501
C10	Capacitor, 15pf	615093-306-501
C11	Capacitor, 100pf	610003-306-501
C12,18	Capacitor, 110pf	611003-306-501
C13	Capacitor, 82pf	682093-306-501
C14,21,45	Capacitor, 240pf	624003-306-501
C15	Capacitor, 27pf	627093-306-501
C16	Capacitor, 150pf	615003-306-501
C17	Capacitor, 220pf	622003-306-501
C19,27	Capacitor, 390pf	639003-306-501
C22,28,40	Capacitor, 270pf	627003-306-501
C23	Capacitor, 180pf	618003-306-501
C24,38	Capacitor, 560pf	656003-306-501
C25	Capacitor, 62pf	662093-306-501
C26,33	Capacitor, 360pf	636003-306-501
C29	Capacitor, 820pf	682003-306-501
C30	Capacitor, 91pf	691093-306-501
C31	Capacitor, 510pf	651003-306-501
C32	Capacitor, 620pf	662003-306-501
C34,42	Capacitor, 1200pf	612013-306-501
C35	Capacitor, 130pf	613003-306-501
C36,37,43	Capacitor, 750pf	675003-306-501
C39	Capacitor, 1600pf	616013-306-501

LOW PASS FILTER
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
C41	Capacitor, 1000pf	610013-306-501
C44	Capacitor. 2400pf	624013-306-501
C46	Capacitor, 1500pf	615013-306-501
C58	Capacitor, 30pf	630093-306-501
CR1-4,7-23	Diode, HP5082	600144-410-001
CR5	Diode, 1N5341B	600026-411-009
L2,7	Inductor, .22µH	600125-376-003
L3	Inductor, .27µH	600125-376-037
L4,30	Inductor, 100µH	600125-376-002
L6,31-34	Inductor, 180µH	600125-376-022
L8,9	Inductor, .33µH	600125-376-001
L10,11	Inductor, .47µH	600125-376-027
L12,13	Inductor, .68µH	600192-376-006
L14,15	Inductor, 1.0µH	600192-376-008
L16,17	Inductor, 1.5µH	600125-376-033
L18,19	Inductor, 2.2µH	600125-376-014
L20	INductor, 2.7µH	600121-376-014
L21	Inductor, 3.3µH	600125-376-006
L22	Inductor, 4.7µH	600125-376-030
L23-29	Inductor, 33µH	600125-376-007
Q1-8	Transformer, 2N2907A	600154-413-001
(Q1-8)	Transformer pad	600025-419-001
R1,2	Resistor, 1K, 1/4W, 5%	610014-341-075
R3,4,30	Resistor, 470K, 1/4W, 5%	647004-341-075
R5-13	Resistor, 10K, 1/4W, 5%	610024-341-075
R14-21	Resistor, 2.2K, 1/4W, 5%	622014-341-075
R22-29	Resistor, 3.3K, 1/4W, 5%	633014-341-075

Figure 5.12 Low Pass Filter Board Assembly



NOTES

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS RATED IN OHMS, 1/4 W, 5%
   ALL CAPACITORS RATED IN PICOFARADS
   ALL INDUCTORS RATED IN MICROHENRYS
   ALL TRANSISTORS ARE 2N2907A
   ALL DIODES ARE HP5082-3188

LAST REF. DESIGNATOR	
C59	Q8
CR23	R30
L34	

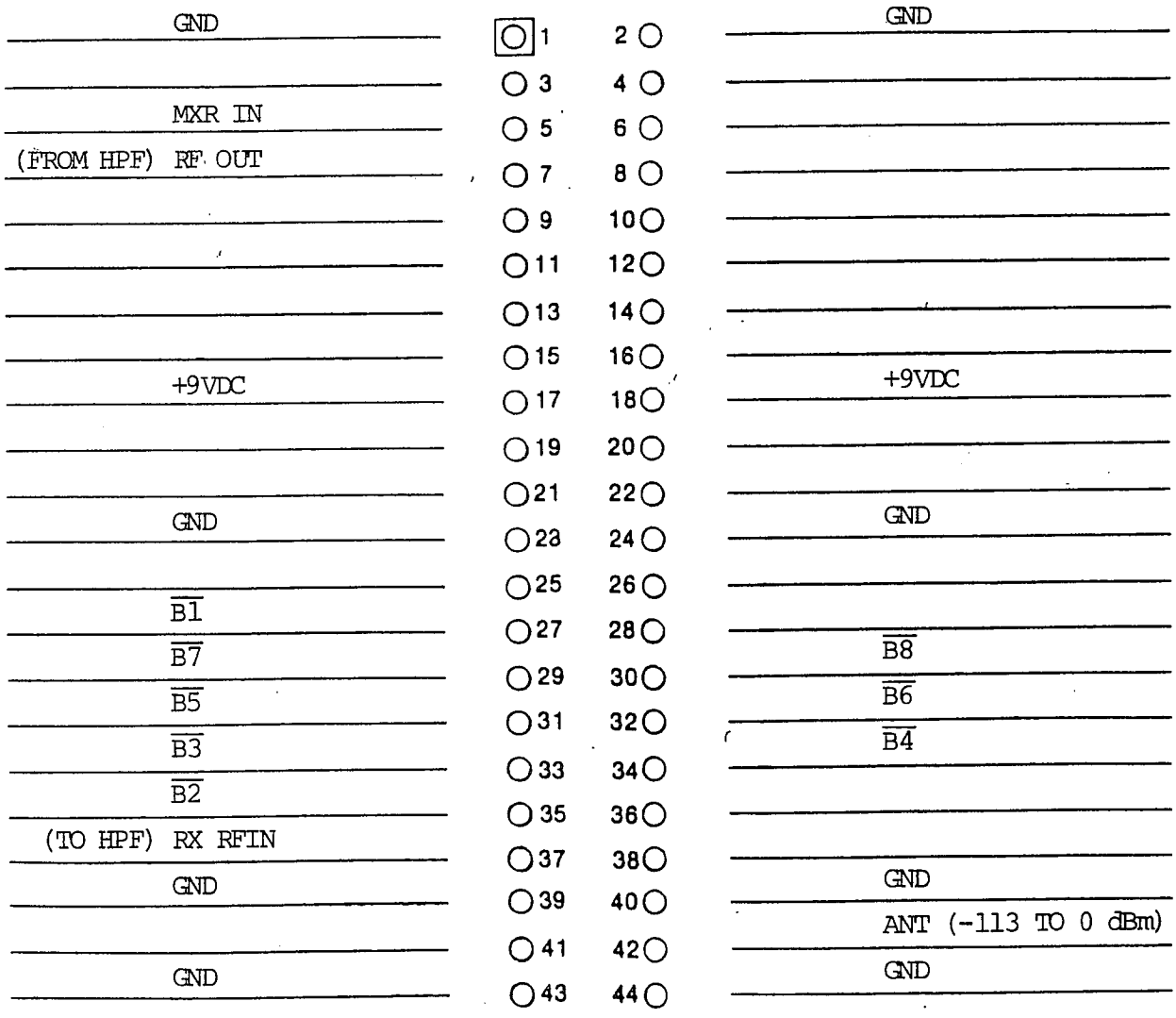
Figure 5.13 Low Pass Filter Board Schematic

LOW PASS FILTER BOARD

1A1A20

PIN CONNECTIONS /VOLTAGE READINGS

1A1A20-J20



BOTTOM VIEW

5.11 HIGH PASS FILTER BOARD, 1A1A18

5.11.1 GENERAL

This board compliments the Low Pass Filter adding preselection and RF amplification. Contained on this assembly are eight (8) elliptical high pass filters with cut-off frequencies of 1.6, 2, 3, 4, 6, 9, 13 and 20 MHz. The desired filter is selected automatically by ground signals from the logic board, 1A1A9. This board also contains a broadcast filter which provides attenuation of greater than 70 dB to broadcast signals (signals below 1.6 MHz), and a very low noise receive RF amplifier. Additional circuitry located on this board provides transmit functions in other applications.

5.11.2 DETAILED DESCRIPTIONS

5.11.2.1 High Pass Filters

Band 1 (B1) is switched by CR1 and CR2. When a logic 0 (ground) is placed on pin 41, Q6 is saturated, and 9 volts appears on the collector of Q6. This voltage causes current to flow through L19, L20, CR1, L18, R50, CR2, L15 and R20. CR1 and CR2 conduct, and all the other band switching diodes (CR3, CR4, CR5 and CR6, etc.) are back-biased. If band 1 is selected, the signal flow is as follows: RF input on pin 42, through K1, C106, CR1, C44, C45, C46, CR2, K1 -pin 8, 2, and through C27 to the broadcast filter. The RF amplifier provides about 4 dB of gain (1.6 -30 MHz). The output is taken from T1 at pin 11 of P14. Operation of any other band is similar. The frequencies at which the various filters are selected, is listed in the table located on the component locations drawing.

5.11.2.2 RF Amplifier

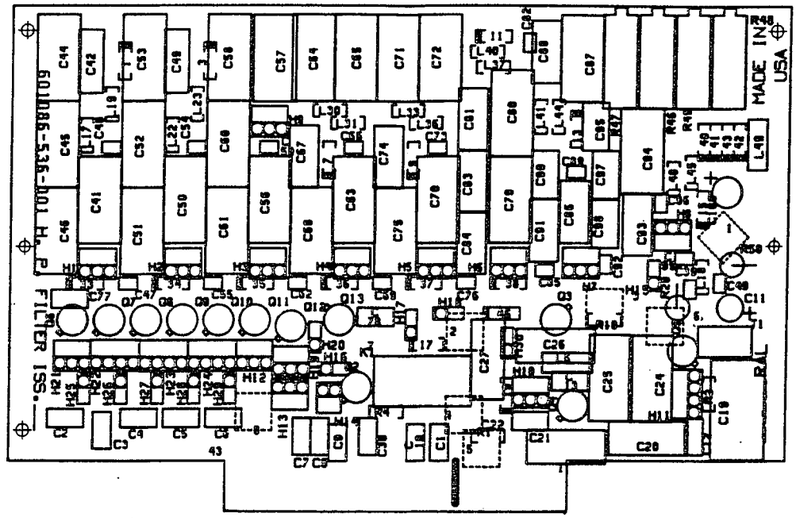
The RF amplifier is used in receive only, and consists of Q4 and Q5. Q5 is a high level FET used in the grounded gate configuration for best intermodulation performance. Q4 is used to provide a constant current source for Q5.

5.11.2.3 Overall Gain

The overall gain is +1 dB to +4 dB, depending on the band selected.

5.11.2.4 Broadcast Filter

The broadcast filter provides approximately 35 dB additional attenuation to the broadcast band. The overall rejection of the broadcast band is approximately 70 dB (6 dB cut-off frequency approximately 1.4 MHz).



HIGH PASS FILTER
(601086-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1-10,12,13, 22,38,77,78	Capacitor, .1µf, 50V	600226-314-008
C11,106	Capacitor, 1µf, elec.	600297-314-003
C19	Capacitor, 5600pf	656013-306-501
C20,65	Capacitor, 820pf	682003-306-501
C21	Capacitor, 1200pf	612013-306-501
C24,25,44,56	Capacitor, 2000pf	620013-306-501
C26,46,50	Capacitor, 3000pf	630013-306-501
C27, C84	Capacitor, 4700pf	647014-306-501
C39,40,47,48, 54,55,59,62, 66,69,73,76, 82,85,89,92, 96,99	Capacitor, .01µf	600268-314-008
C41	Capacitor, 4000pf	640011-306-501
C42	Capacitor, .012µf	600204-314-022
C45	Capacitor, 1300pf	613014-306-501
C49	Capacitor, .01µf	600204-314-001
C51	Capacitor, 2200pf	622014-306-501
C52,58,68,	Capacitor, 1000pf	610013-306-501
C53,63	Capacitor, 1600pf	616014-306-501
C57	Capacitor, 6200pf	662014-306-501
C60	Capacitor, 707pf	670703-306-501
C81	Capacitor, 1400pf	614013-306-501
C87	Capacitor, 500pf	650001-306-501
C70	Capacitor, 1100pf	611013-306-501
C71	Capacitor, 3300pf	633014-306-501
C72	Capacitor, 560pf	656003-306-501
C74,91	Capacitor, 360pf	636003-306-501
C75,79	Capacitor, 750pf	675003-306-501
C80	Capacitor, 2100pf	621011-306-501

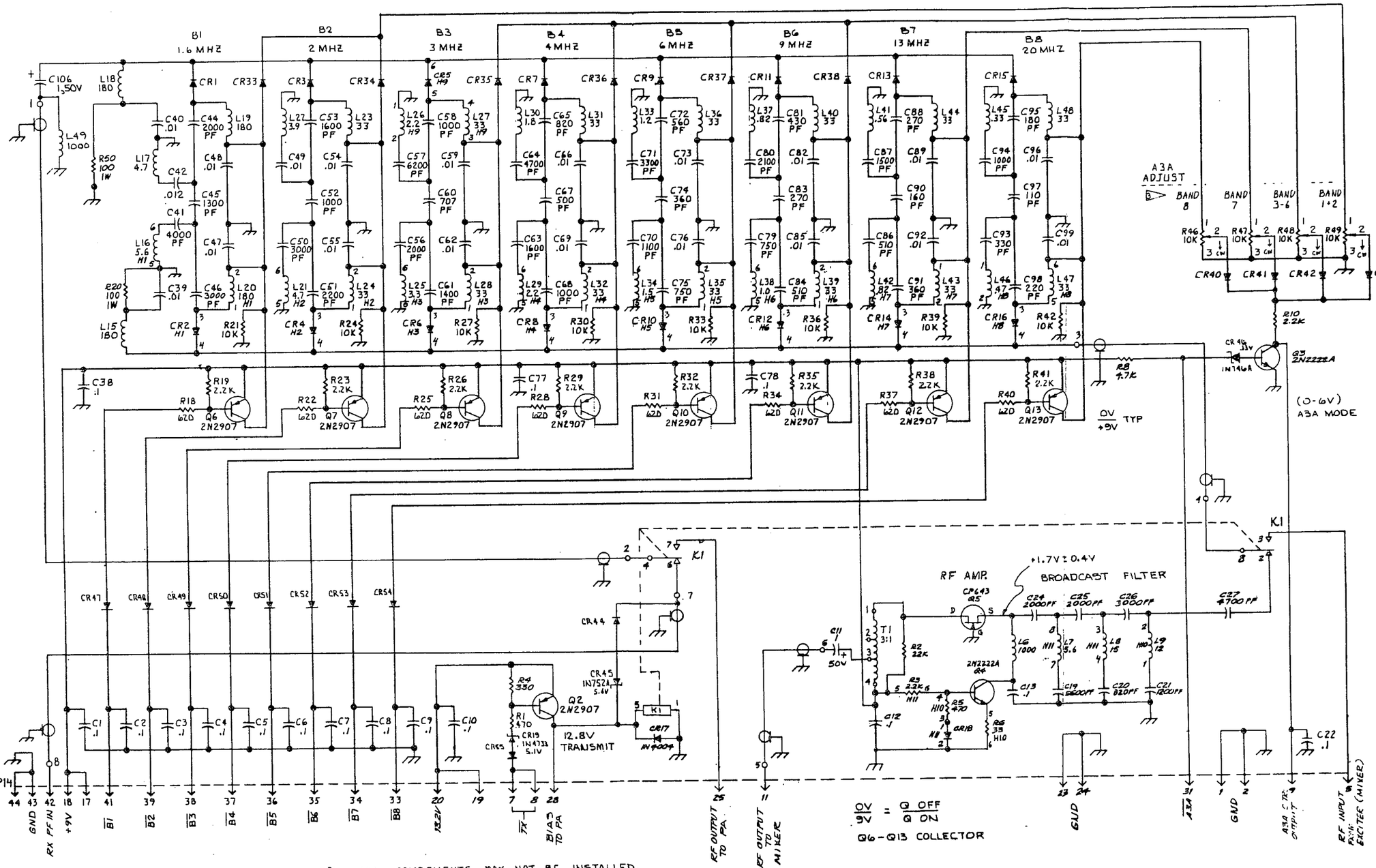
HIGH PASS FILTER
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
C81	Capacitor, 430pf	643003-306-501
C83,88	Capacitor, 270pf	627003-306-501
C84,86	Capacitor, 510pf	651004-306-501
C87	Capacitor, 1500pf	615013-306-501
C90	Capacitor, 160pf	616003-306-501
C93	Capacitor, 330pf	633003-306-501
C94		
C95	Capacitor, 180pf	618004-306-501
C97	Capacitor, 110pf	611004-306-501
C98	Capacitor, 220pf	622003-306-501
CR1-16	Diode, HP3188	600144-410-001
CR17	Diode, 1N4004	600011-416-002
CR18,33-38 40-44,47-55	Diode, 1N4148	600109-410-001
CR19	Diode, 1N4733	600006-411-006
CR45	Diode, Zener 5.6V 1N752A	600002-411-007
CR46	Zener, 1N746A, 3.3V	600002-411-001
K1	Relay, 12V	600028-402-006
L6,49	Choke, 1000µH	600034-376-001
L7,16	Choke, 5.6µH	600125-376-043
L8	Choke, 15µH	600125-376-013
L9	Choke, 12µH	600125-376-020
L15,18-20	Choke, 180µH	600125-376-022
L17,21	Choke, 4.7µH	600125-376-030
L22	Choke, 3.9µH	600125-376-018
L23,24,27,28, 31,32,35,36, 39,40,43,44, 47,48	Choke, 33µH	600125-376-007

HIGH PASS FILTER
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
L25	Choke, 3.3µH	600125-376-008
L26,29	Choke, 2.2µH	600125-376-016
L30	Choke, 1.8µH	600125-376-017
L33	Choke, 1.2µH	600125-376-041
L34	Choke, 1.5µH	600125-376-033
L37,42	Choke, .82µH	600125-376-039
L38	Choke, 1.0µH	600125-376-040
L41	Choke, .56µH	600125-376-005
L45	Choke, .33µH	600125-376-001
L46	Choke, .47µH	600125-376-027
Q2,6-13	Transistor, 2N2907A	600154-413-001
Q3,4	Transistor, 2N2222A	600080-413-001
Q5	Transistor, CP643	600340-413-001
R2	Resistor, 22K, 1/4W, 5%	622024-341-075
R3,10	Resistor, 2.2K, 1/4W, 5%	622014-341-075
R4	Resistor, 330Ω, 1/4W, 5%	633004-341-075
R5,1	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R6	Resistor, 33Ω, 1/4W, 5%	633094-341-075
R8	Resistor, 4.7K, 1/4W, 5%	647014-341-075
R18,22,25, 28,31,34, 37,40,	Resistor, 620Ω, 1/4W, 5%	662004-341-075
R19,23,26, 29,32,35, 38,41	Resistor, 2.2KΩ, 1/4W, 5%	622014-341-075
R20,50	Resistor, 100Ω, 1W, 5%	610004-341-325
R21,24,27, 30,33,36, 39,42	Resistor, 10KΩ, 1/4W, 5%	610024-341-325
R46-49	Resistor, 10K, variable	600063-360-010
T1	Transformer	600148-512-001

Figure 5.14 High Pass Filter Board Assembly



NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTORS ARE IN OHMS, 1/4W, 5%
   CAPACITORS ARE IN MFD
   INDUCTORS ARE IN μHY.
2. DIODE CR17 IS IN4004, CR1-16 ARE HP3188, CR19 IN4728, ALL OTHERS ARE IN4148

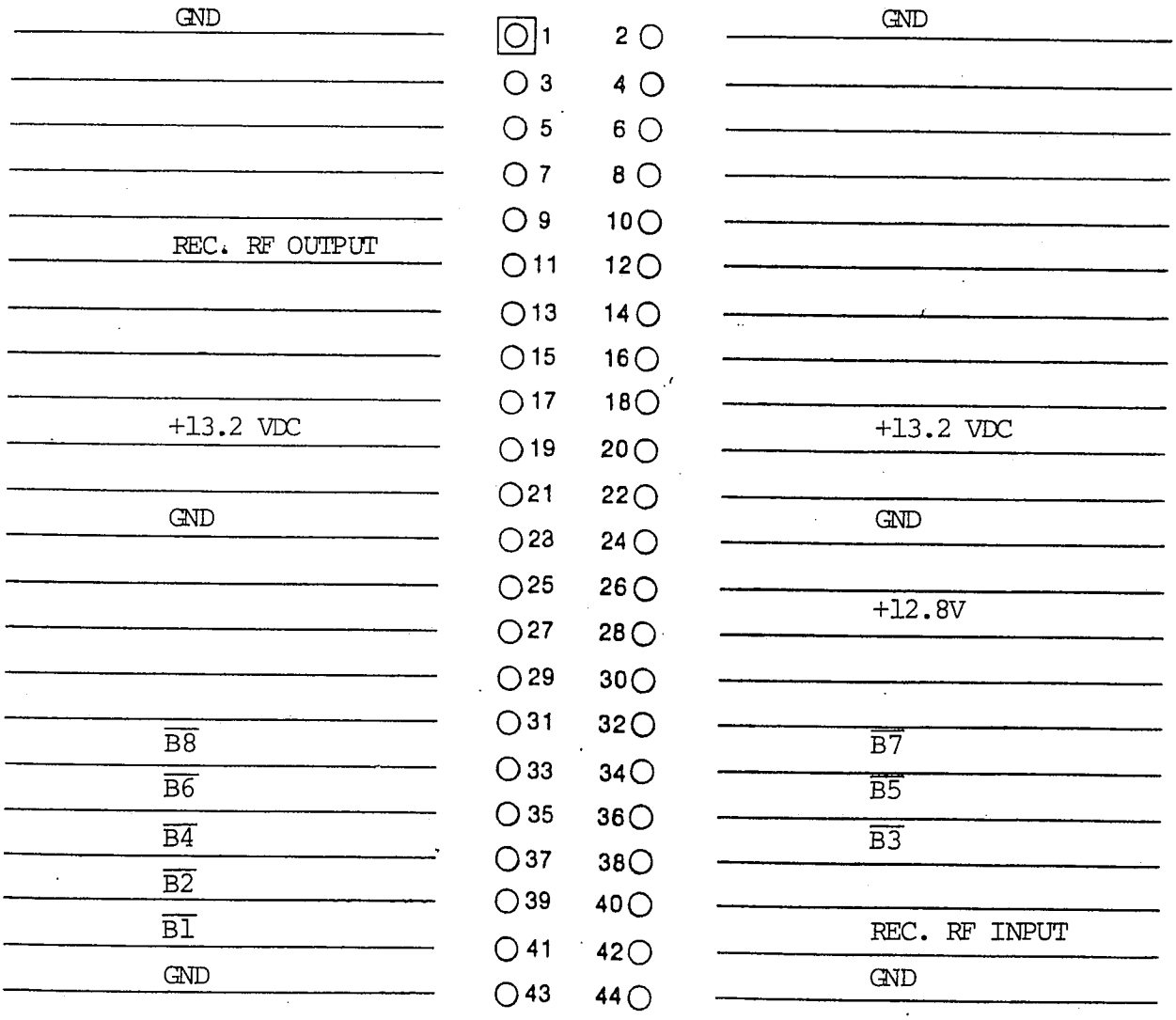
Figure 5.15 High Pass Filter Board Schematic

HIGH PASS FILTER BOARD

1A1A18

PIN CONNECTIONS/VOLTAGE READINGS

1A1A18-J18



BOTTOM VIEW

5.12 MIXER BOARD, 1A1A16

5.12.1 GENERAL

The Mixer Board figures 5.20 and 5.21 performs all the major frequency conversions in the receiver. .01 to 30 MHz signals from the low pass filter, 1A1A20, are applied to a high dynamic range double balanced mixer. The received signal is combined with the first LO signal (59.63 - 89.53 MHz) from the major loop board, 1A1A15 (part of the synthesizer), to form a VHF first IF frequency of 59.53 MHz. The signal then passes through a monolithic filter, allow noise FET amplifier and a second monolithic 59.53 filter before being applied to a second double balanced mixer.

In this mixer, the 59.53 MHz first receive IF is mixed with a 54.53 MHz second local oscillator from the translator loop board, 1A1A13 (part of the synthesizer), to obtain a second receive IF signal of 5.0 MHz, which is then applied to the IF filter board, 1A1A14 via buffer amplifier on the mother board.

To enhance the excellent dynamic range of the receiver, a delayed AGC voltage from the audio squelch board, 1A1A10, is applied to the receive VHF IF amplifier stage, located on this board, to reduce the receiver gain under conditions of very strong input signals.

5.12.2 DETAILED DESCRIPTIONS

5.12.2.1 First LO Amplifier

The first LO is applied to P16, pin 3 and then to Q8. The first LO amplifier consists of C39, R24, R23, Q8, T4 and associated components. The input is 0 dBm and is amplified to +4 dBm in Q8. R23, R25, C40, L14 and C41 form a "peaking network" in the emitter circuit to flatten the gain from 59.63 - 89.53 MHz.

T4 matches the collector impedance of Q8 to the input of the first mixer. C38, L13 and C37 provide RF isolation from the first LO amplifier to the remaining circuitry.

5.12.2.2 Second LO Amplifier

The second LO is fed to P16, pin 41 at 0 dBm and is amplified to +4 dBm by Q1. The second LO amplifier (54.53 MHz) consists of C4, R4, R5, Q1, T1 and associated circuitry. Q2 is a noise blanker switch used in other applications.

5.12.2.3 Receive Input Low Pass Filter

The receive input (pin 12) is fed through the input filter (118, L19, C57, C58, CR5, CR6, CR7 and etc.) to the middle of T3. This filter has a cut off frequency of 31 MHz and is also used as a variable attenuator. Diodes CR5, CR6, CR7 and Q15 are used to attenuate the input signal before it gets to the first mixer.

5.12.2.4 Delayed AGC Circuit

The delayed AGC is applied to pin 39 and 40 and reduces the DC level to gate 2 of the receive (Q5) bilateral amplifier. Also, the delayed AGC voltage causes Q15 to conduct, causing current to flow through CR5, CR6 and CR7. This current causes a loss through L18 and L19. It should be noted that current does not flow through the attenuator diodes (CR5, CR6 and CR7) until Q15 emitter falls to below about +4.6 VDC (note CR3 and R10 divider). The delayed AGC allows signals of .2 VP-P to be received with an IMD (in band) of -30 dBm.

5.12.2.5 Transistors Q9 and T3

Q9 is saturated by a DC voltage, applied to P16, pin 4, via CR4, and R28. An AC ground is thereby placed on pin 3 of T3 and the receive

signal, applied to pin 2 of T3, is stepped up 2:1 in T3. Pin 1 of T3 couples the receive signal, via C7, to the input of the first mixer, M2.

5.12.2.6 First Mixer

The receive input is applied to pin 1 of mixer M2. The first LO is applied to pin 8. The translated frequency (59.53 MHz) comes from pin 3 and 4 of M2. L8, C33 and C34 matches the impedance of the monolithic filter FL2, (1000 ohms) to the output impedance of the mixer (50 ohms). The output of FL2 is fed to C31 and L6 through C27 to gate 1 of Q5. Q5 is the receive portion of the bi-lateral amplifier.

5.12.2.7 Bi-Lateral Amplifier

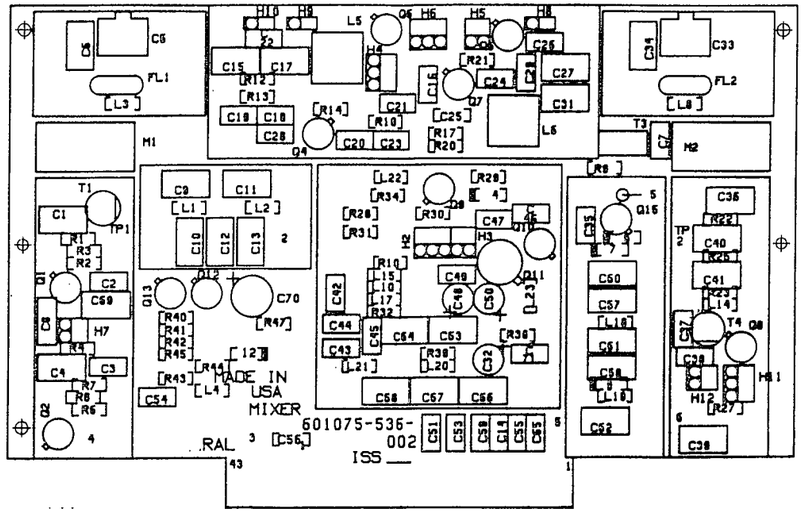
The receive amplifier is Q5. Q7 is saturated during the receive mode by the collector of Q12. When Q7 is saturated (the collector voltage of Q7 is near 0 when saturated), Q5, source and drain current can flow and Q5 amplifies its gate 1 voltage. Gate 2 is the delayed AGC and as it is lowered, the gain of Q5 decreases. The output of Q5, is developed across L5 and C15 (resonant at 59.53 MHz). Q5, L5 and C15 have about +20 dB voltage gain. However, because of the loss of M2, F12, F11 and M1, the overall receive gain is near 0 dB.

5.12.2.8 FL1 and Matching

The output of L5 and C15 is matched to the input Z of FL1 (approximately 1000 ohms). The output of FL1 is matched to a lower Z of M1 by C6 and L3. The receive input is applied to pin 1 of M1 and converted to 5,000 MHz when mixed with the second LO (54.53 MHz).

5.12.2.9 Output Filter

The output low pass filter (L1, L2, C9, C11, etc.) removes the second LO and the first LO component before the receive signal is applied to the IF/filter board (Filter cut off frequency is approximately equal to 30 MHz).



MIXER BOARD
(601075-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1,4,36,39, 40,69	Capacitor, 180pf, mica	618003-306-501
C2,3,7,16,14, 26,18-24,28, 29,35,37,38, 42-47,49,51, 53-55,59,65, 71	Capacitor, .1µf, mono	600226-314-008
C5,33	Capacitor, 9-35pf, variable	600018-317-013
C6,34	Capacitor, 20pf, mica	620093-306-501
C8	Capacitor, 47pf, NPO	600269-314-022
C9,58	Capacitor, 15pf, mica	615091-306-501
C10,62	Capacitor, 82pf, mica	682093-306-501
C11,17,27,57	Capacitor, 47pf, mica	647093-306-501
C12,61	Capacitor, 130pf, mica	613003-306-501
C13,60	Capacitor, 68pf, mica	668093-306-501
C15,31	Capacitor, 5.6pf, mica	656081-306-501
C25,56	Capacitor, .001µf, 50V	600272-314-008
C32,48,50	Capacitor, 1µf, 50V	600297-314-003
C41	Capacitor, 27pf, mica	627093-306-501
C63	Capacitor, 18pf, mica	618091-306-501
C64	Capacitor, 51pf, mica	651093-306-501
C66	Capacitor, 100pf, mica	610003-306-501
C67	Capacitor, 160pf, mica	616004-306-501
C68	Capacitor, 75pf, mica	675093-306-501
C70	Capacitor, 220µf, 10V	600297-314-037
CR4,9	Diode, 1N4148	600109-410-001

MIXER BOARD
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
CR5,6,7	Diode, KS1001	600179-410-001
CR10	Diode, HP5082-3080	600156-410-001
CR11	Diode, 1N5230B	600033-411-010
FL1,2	Filter, 59.53 MHz	600060-529-004
L1,19,20	Choke, .27µH	600125-376-037
L2,18	Choke, .18µH	600125-376-031
L3	Choke, .82µH	600125-376-039
L4	Choke, 33µH	600125-376-007
L5,6	Choke, .33µH, variable	600169-376-001
L8	Choke, .82µH	600125-376-040
L9,11,12,13	Choke, 3.3µH	600125-376-006
L10	Choke, 10µH	600125-376-032
L16	Choke, 4.7µH	600125-376-030
L14	Choke, .1µH	600125-376-028
L21	Choke, .22µH	600125-376-003
L23	Choke, 15µH	600125-376-013
L15,17,22	Choke, 180µH	600125-376-022
M1,2	Mixer, SRA-3H	600007-455-001
Q1,2,4-10,12, 13,15	Transistor pad (T018)	600025-419-001
Q1,8,10	Transistor, 2N918	600085-413-001
Q,6,7,9	Transistor, 2N2222A	600080-413-001
Q4,5	Transistor, 40822	600276-413-001
Q11	Transistor, 2N3866	600134-413-001

MIXER BOARD
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
(Q11)(T1,T4)	Transistor pad (T05)	600017-419-001
Q12,13,15	Transistor, 2N2907A	600154-413-001
R1,6,27	Resistor, 51Ω, 1/4W, 5%	651094-341-075
R2,23	Resistor, 15Ω, 1/4W, 5%	615094-341-075
R3	Resistor, 160Ω, 1/4W, 5%	616004-341-075
R4,20,26,34	Resistor, 3.9K, 1/4W, 5%	639014-341-075
R7	Resistor, 22K, 1/4W, 5%	622024-341-075
R8,12,16,17, 21,28,29,45,50	Resistor, 10K, 1/4W, 5%	610024-341-075
R10	Resistor, 360Ω, 1/4W, 5%	636004-341-075
R13	Resistor, 12K, 1/4W, 5%	612024-341-075
R14,19	Resistor, 47K, 1/4W, 5%	647024-341-075
R15,39	Resistor, 10Ω, 1/4W, 5%	610094-341-075
R18	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R22,36,47	Resistor, 220Ω, 1/4W, 5%	622004-341-075
R25,48,49	Resistor, 82Ω, 1/4W, 5%	682094-341-075
R32,42,44	Resistor, 2.7K, 1/4W, 5%	627014-341-075
R33	Resistor, 1K, 1/4W, 5%	610014-341-075
R35,38	Resistor, 8.2Ω, 1/4W, 5%	682084-341-075
R37,40	Resistor, 3.3K, 1/4W, 5%	633014-341-075
R41,43,31	Resistor, 330Ω, 1/4W, 5%	633004-341-075
R51	Resistor, 300Ω, 1/4W, 5%	630004-341-075
R59,24,30	Resistor, 4.7K, 1/4W, 5%	647014-341-075
T1,4	Transformer, 3:1	600094-512-001
T3	Transformer, toroid	600091-512-001
TP1,2	Terminal	600284-230-002

Figure 5.16 Mixer Board Assembly

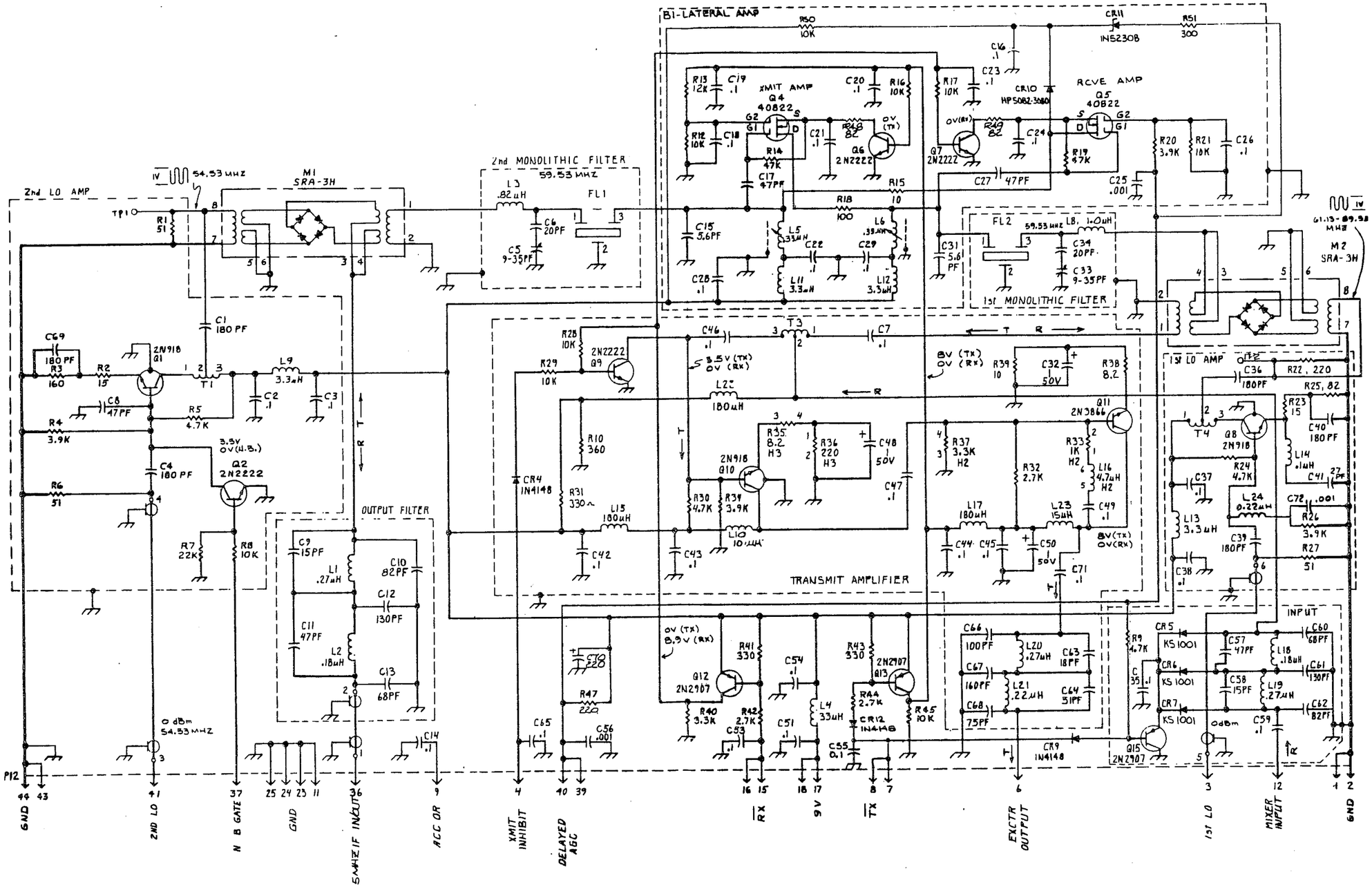


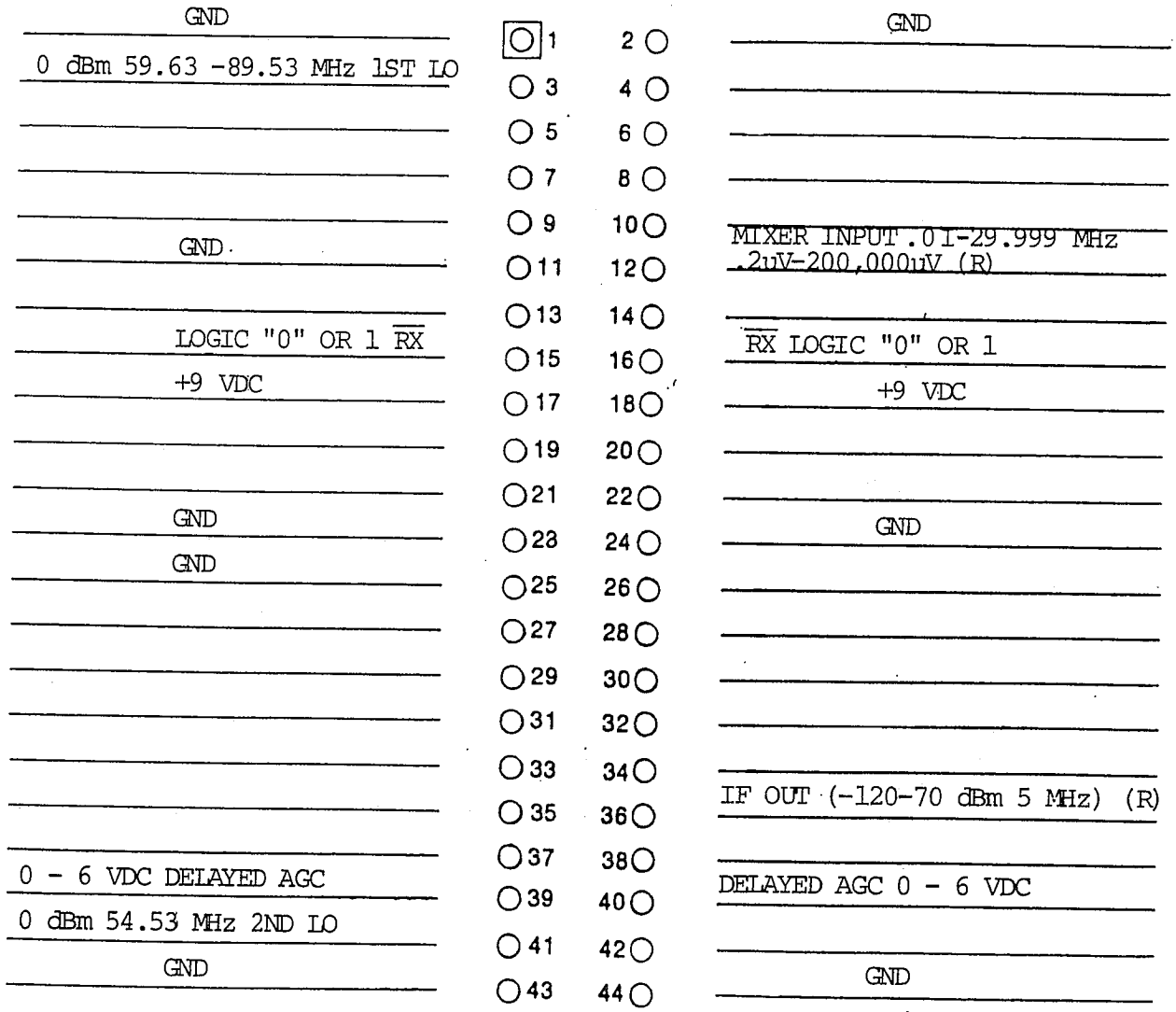
Figure 5.17 Mixer Board Schematic

MIXER BOARD

1A1A16

PIN CONNECTIONS/VOLTAGE READINGS

1A1A16-J16



BOTTOM VIEW

5.13 IF FILTER BOARD, 1A1A14

5.13.1 GENERAL

The IF filter board contains the three 5 MHz information filters and amplifiers. These filters are: FL1 - upper sideband operation, FL2 - lower sideband operation and FL3 - AM operation. The appropriate filter is selected by diode switching via mode information from the interface board, 1A1A1. A 5 MHz IF signal from the mixer board, 1A1A16, is passed through the appropriate IF filter and further amplified in three stages. The gain of the IF output is adjustable. An AGC voltage is applied from the audio squelch board, 1A1A10, to two of the IF amplifier stages to reduce the IF gain on very strong received signals.

Other circuits on this board are used in transmit functions in other applications. Figures 5.22 and 5.23 show the assembly and schematic of this board.

5.13.2 DETAILED DESCRIPTION

5.13.2.1 Filter Selection

The filters are selected by placing a ground (logic 0) on certain pins on the connector. FL1 is used to receive USB. (The pass band is on the lower side of 5 MHz, but the signal is transferred to the high side in the mixer.) When USB is selected, ground is placed on pin 35. This action causes current to flow through R36, CR10, L14 and CR4. Diode CR10 is connected to the common receive input line (CR3, C20) and when it conducts, the signal is applied to the input to FL1. In a similar manner, the ground on pin 35 causes current to flow through R37, CR13, L19, L11 and CR4. When CR13 is conducting, the output of FL1 is connected to the common output line (C35, CR15 and CR17).

It should be noted that CR11 and CR12, used to short out the filter input and output if the filter is not selected, are cut off by R35 and R20. When FL1 is not selected, current through R23, CR11 and CR12 shorts out the filter input and output. Note also, when FL1 is selected, FL2 and FL3 are shorted out. FL2 is selected on pin 37 (LSB). FL3 is selected by a ground on pin 31 (AM). The ground on pin 31 causes Q5 to conduct, selecting the AM filter.

5.13.2.2 Receive Path

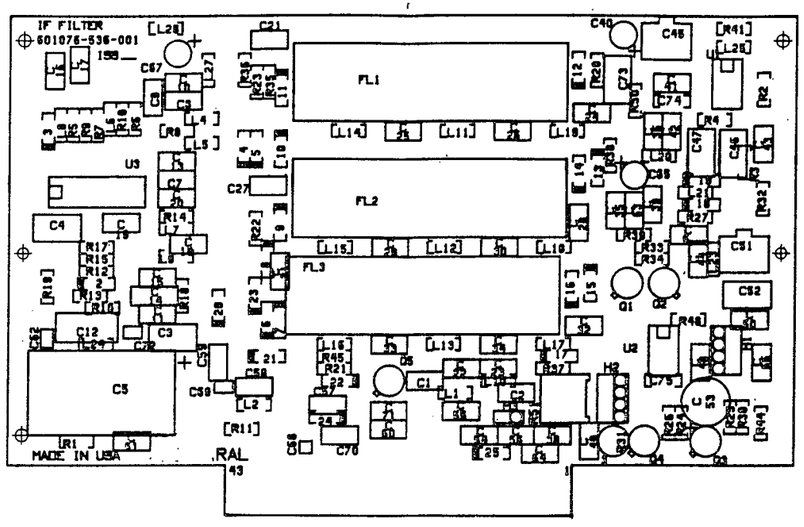
The receive input is on pin 36. The input of U3C is matched to 50 ohms by L2 and C3. The signal is amplified by U3C and U3D, the gain of this combination is approximately 20 dB. An ISB output is provided on pin 41 through R1 and C61. The output of U3D is fed through R10, C16 and CR3 to the inputs of the filters. R10 is selected to provide a 50 ohm driving source for the filters. R19 is connected to receive +9 volts through L8 and determines the amount of turn on current through CR3. C4 is used to cancel some inductive reactance and compensate the driving impedance for the filters. The amplified input signal passes through CR3 and the selected filter.

At the output of the filters, the signal passes through C35 and CR19 into the input of U1, the first receive amplifier. R38 determines the turn on current for C19. C73 is a compensating capacitor to provide a 50 ohm load for the filter termination. (C63 and R39 provide the primary filter terminating impedance.)

The filter output is amplified in U1 and U2, which are AGC controlled. The AGC input is applied to pin 12. As pin 12 voltage is increased above +4 VDC, the gain is decreased. The output from U2 is fed to Q3 and Q4 for further amplification. The overall receive gain is set by adjusting R31. 50 µV input will provide 100,000 µV output at pin 5. In the transceiver, R31 is adjusted to have an AGC threshold of 6 to 8 microvolts input to the receiver. The precise setting of R31 is therefore a function of the receiver front end gain.

5.13.2.3 Miscellaneous Circuitry

Q1 is the transmit switch and is activated when a logic 0 is placed on pin 7. The collector of Q1 rises to +9 volts and conditions the board for transmit operation. In a similar manner, a logic 0 on pin 16 causes +9 volts on the collector of Q2 and the board is conditioned for receive/receive operation. Capacitors, such as C62, C72, C55, C54, etc. are RF bypasses. L24 is used in the TGC line to prevent feedback from the PA causing transmitter loop oscillation.



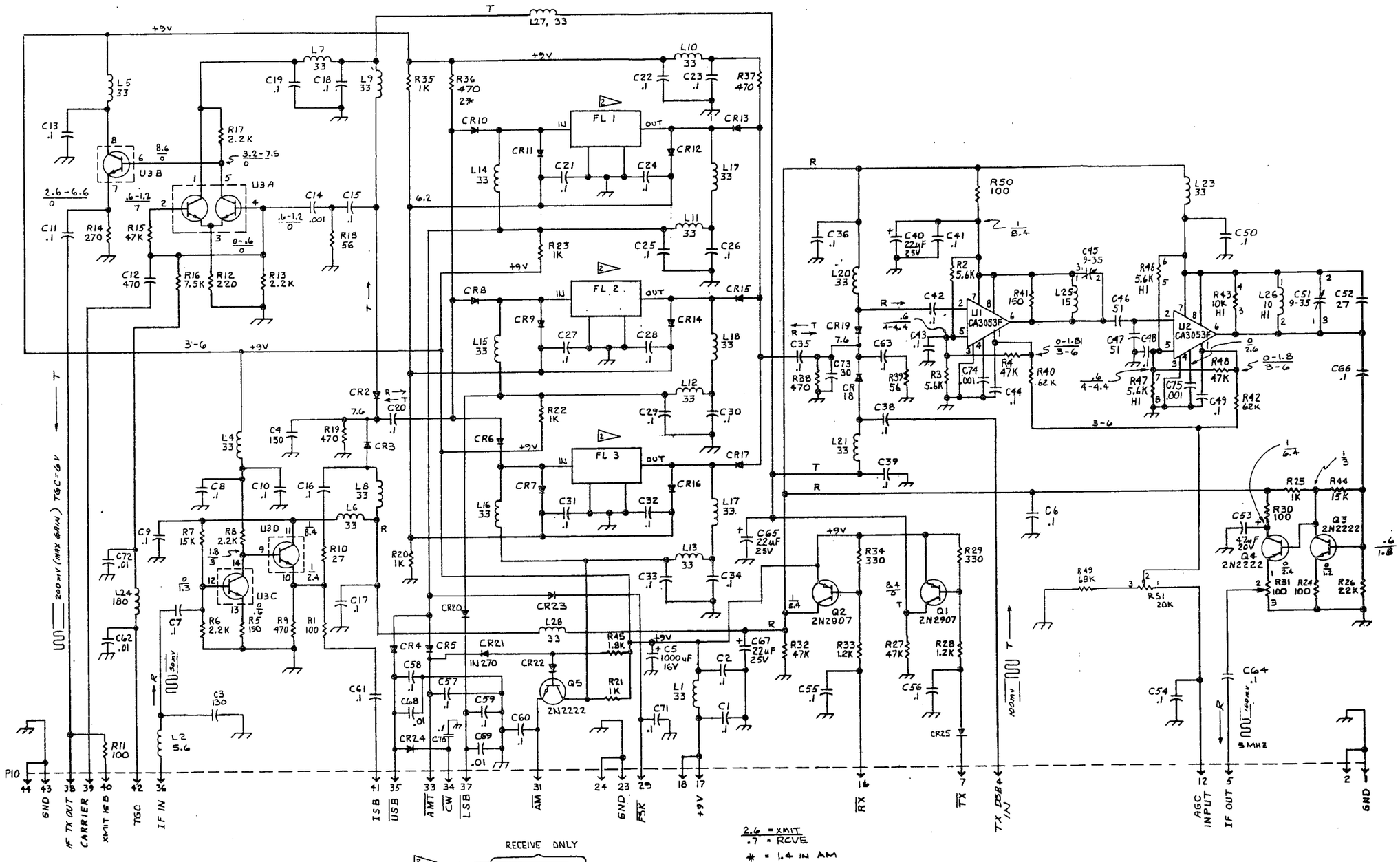
FILTER/IF AMPLIFIER
(601076-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1,2,6-11, 13,15-36, 38,39,41-44,48-50, 54-61,63, 64,66,70, 71	Capacitor, .1µf, 50V	600226-314-008
C3	Capacitor, 130pf	613003-306-501
C4	Capacitor, 150pf	615003-306-501
C5	Capacitor, 1000µf, 16V	600259-314-007
C12	Capacitor, 470pf	647003-306-501
C14	Capacitor, .001µf	600189-314-014
C40,65,67	Capacitor, 22µf, 25V	600297-314-016
C45,51	Capacitor, 9-35pf, variable	600018-317-013
C46,47	Capacitor, 51pf	651093-306-501
C52	Capacitor, 27pf	627094-306-501
C53	Capacitor, 47µf, 20V	600297-314-026
C62,68,69, 72	Capacitor, .01µf, 50V	600268-314-008
C73	Capacitor, 30pf	630094-306-501
C74,75	Capacitor, .001µf, 50V	600272-314-004
CR2-20,22, 23,24,25	Diode, 1N4148	600109-410-001
CR21	Diode, 1N270	600052-410-001
FL1(LSB)	Crystal, filter	600083-529-001
FL1(USB)	Crystal, filter	600084-529-001
FL2(LSB)	Crystal, filter	600083-529-001
FL3	Crystal, filter	600082-529-001
H3	Vert. mount, 1 pos.	600064-419-005
L1,4-21, 23,27,28	Choke, 33µH	600125-376-007
L2	Choke, 5.6µH	600125-376-043
L24	Choke, 180µH	600125-376-022

FILTER/IF AMPLIFIER
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
L25	Choke, 15µH	600125-376-013
L26	Choke, 10µH	600125-376-032
Q1,2	Transistor, 2N2907A	600154-413-001
Q3,4,5	Transistor, 2N2222A	600080-413-001
R1,11,24, 30,50	Resistor, 100Ω, 1/4W,5%	610004-341-075
R2,3,46, 47	Resistor, 5.6K	656014-341-075
R4,15,27, 32,48	Resistor, 47K, 1/4W,5%	647024-341-075
R6,8,13,17	Resistor, 2.2K, 1/4W, 5%	622014-341-075
R7,44	Resistor, 15K, 1/4W, 5%	615024-341-075
R9,19,36-38	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R10	Resistor, 27Ω, 1/4W, 5%	627094-341-075
R12	Resistor, 220Ω, 1/4W, 5%	622004-341-075
R14	Resistor, 270Ω, 1/4W, 5%	627004-341-075
R16	Resistor, 7.5K, 1/4W, 5%	675014-341-075
R18,39	Resistor, 56Ω, 1/4W, 5%	656094-341-075
R20-23,25, 35	Resistor, 1K, 1/4W, 5%	610014-341-075
R26	Resistor, 22K, 1/4W, 5%	622024-341-075
R28,33	Resistor, 1.2K, 1/4W, 5%	612014-341-075
R29,34	Resistor, 330Ω, 1/4W, 5%	633004-341-075
R31	Resistor, 100Ω, Var.	600061-360-004
R40,42	Resistor, 62KΩ, 1/4W, 5%	662024-341-075
R41,5	Resistor, 150Ω, 1/4W, 5%	615004-341-075
R43	Resistor, 10K, 1/4W, 5%	610024-341-075
R45	Resistor, 1.8K, 1/4W, 5%	618014-341-075
R49	Resistor, 68K, 1/4W, 5%	668024-341-075
R51	Resistor, 20KΩ, Var.	600072-360-011
U1,2	IC, CA3053F	600270-415-001
U3	IC, CA3045	600038-415-001
	Untested filt. IF amp	601076-536-951
	Untested,filt. IF amp	601076-536-952

Figure 5.18 IF Filter Board Assembly



	-001	-002	-003	-004
FL1	USB	LSB	LSB	USB
FL2	LSB	VACANT	CW 1KHZ	AM 12KHZ
FL3	AM 6KHZ	VACANT	CW 400HZ	AM 6KHZ

NOTES:
1. UNLESS OTHERWISE NOTED: RESISTOR ARE IN OHMS, 1/4W, ±5%; CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS (pF), VALUES LESS THAN ONE ARE MICROFARARADS (μF); CHOKES ARE IN MICROHENRIES (μH); U3 IS A CA3045; DIODES ARE IN4148.

Figure 5.19 IF Filter Board Schematic

IF FILTER BOARD

1A1A14

PIN CONNECTIONS/VOLTAGE READINGS

1A1A14-J14

(MULTI-USE BOARD: (XXXX) = PIN FUNCTION IN THIS APPLICATION;
N.C. = NO CONNECTION)

GND	1	GND
	3	TX DSB IN 100 mVPP (N.C.)
100 mVPP IF OUT	5	
(N.C.) LOGIC "0" OR 1 TX	7	
	9	
	11	AGC INPUT +3 - +6 VDC (R)
	13	
	15	$\overline{RX}$ LOGIC "0" OR 1 (GND)
+9 VDC	17	+9VDC
	19	
	21	
GND	23	GND
	25	
	27	
(N.C.) LOGIC "0" OR 1 $\overline{FSK}$	29	
($\overline{WIDE}$) LOGIC "0" OR 1 $\overline{AM}$	31	
($\overline{MED}$) LOGIC "0" OR 1 $\overline{AMT}$	33	$\overline{CW}$ LOGIC "0" OR 1 ($\overline{ISB}$)
LOGIC "0" OR 1 $\overline{USB}$	35	REC. IF IN 50 mVPP
LOGIC "0" OR 1 $\overline{LSB}$	37	5 MHz TX IF OUT 200 MvPP (T) (N.C.
(N.C.) (AMT) -18-25 dBm 5 MHz	39	ISB IF OUT 200 mVPP (T) (N.C.)
ISB OUT	41	TGC +2.9 - +3.9 VDC (T) (N.C.)
GND	43	GND

1	2
3	4
5	6
7	8
9	10
11	12
13	14
15	16
17	18
19	20
21	22
23	24
25	26
27	28
29	30
31	32
33	34
35	36
37	38
39	40
41	42
43	44

BOTTOM VIEW

5.14 AUDIO/SQUELCH BOARD, 1A1A10

5.14.1 GENERAL

The audio/squelch board, Figures 5.24 and 5.25, accepts the 5 MHz IF output from the IF filter board, 1A1A14, and performs the final detector function to convert the intermediate frequency signal into usable audio intelligence. This process involves two discrete, but not simultaneous, detector functions. A product detector is operative in all modes except the AME mode. In the AME mode, an envelope detector is operative. Two separate audio outputs are provided. A 600 ohm line audio output is applied to the rear panel connector, 1A22J42, and a low level output is applied to the speaker/amplifier board, 1A1A34, to provide the front panel speaker and headphones/headset audio.

Located on this board are an input IF amplifier, AGC detector and amplifier, AM/product detector, squelch amplifiers and gating circuitry. (In the AME mode, AGC voltage is derived from the 5 MHz carrier by CR3 and CR4. In CW, SSB and FSK modes, AGC is derived from the detected audio.) Fast attack fast decay is used for AM and FSK signals, and fast attack slow decay is used for sideband and CW signals. AGC voltage to the IF filter board, 1A1A14, and delayed AGC voltage to the mixer board, 1A1A16, controls the receiver gain.

Other circuitry and functions through this board are side tone and mute functions. The rear panel audio (600 ohm) is unaffected by operation of the squelch control.

5.14.2 DETAILED DESCRIPTIONS

5.14.2.1 Input IF Amplifier and AGC Amplifier

Q2 is an input amplifier that accepts the IF input on pin 5, amplifies and drives Q10, an emitter follower. The follower is used to provide a low driving impedance for the AGC detector and the product detector. The output of Q10 is rectified in the voltage doubler C4, CR3 and CR4. The rectified DC, applied between the emitter and base of Q3, causes Q3 to conduct, causing current to flow through R1 and R5. The positive going emitter voltage of Q3 is fed through CR17 to pin 11. This AGC voltage is used to reduce the gain of the IF filter board. The AGC voltage drives Q1 through R5, generating a negative going delayed AGC on pin 40. The delayed AGC is used to control the gain of the mixer and is used for large input signals. R5 is adjusted so Q1 collector voltage is 7 VDC when a signal is applied at the antenna to produce 4.4 VDC AGC voltage.

5.14.2.2 Product Detector and AM Detector

The product detector consists of U1A, U1B and U1C. The output of Q10 is fed through C17 to pin 2 of U1A. The third LO, from pin 12, is applied via C16, to the base (pin 12) of U1C. Since U1A emitters are connected in series with U1C, the third LO modulates the current through U1A, causing a mixing action. Audio voltage is developed in the collector circuit (pin 5) and the 5 MHz is filtered by C19.

The detected audio is fed through U1B and U1D to drive other circuits. It should be noted that in USB or LSB, the collector load for U1A is R23 in parallel with R22. A logic 0 on pin 35 or 37 will cause Q6 to conduct, applying +9 volts through CR7 and R23. During AM operation, Q6 is cut off and the collector load for U1A is R22 only. Also, the third LO input is attenuated 40 dB. For AM detection U1A operates as an envelope detector. When Q6 is cut off, R18 causes current to flow through CR1 and R13. This action further reduces the amount of the third LO present during AM operation.

5.14.2.3 600 Ohm Line Driver

The product detector/AM detector output is fed through emitter follower U1B to C39 and R54. R54 is adjusted to provide the proper output on pin 14 and pin 6. The output of R54 is fed through C40 and R53 to pin 6 of U4A. U4A and Q7 further amplify the signal and the floating 600 ohm output is developed across T1 pin 1 and 3. It should be noted that the DC input to transformer T1 is on pin 5. Q7 current flowing from pin 5 to 4 is balanced by R42 current flowing from pin 5 to 6. This configuration prevents T1 from being saturated by the DC current of T1. The nominal output of the line driver is 0 dBm, but is adjustable to +10 dBm.

5.14.2.4 Squelch Amplifier

The squelch amplifier consists of C20, R25, U4B, Q8, CR9, CR10 and associated components. The audio output from U1B drives through C40 and R25 to pin 3 of U4B. U4B is operated as a variable gain amplifier. The gain variation is achieved by removing negative feedback (reducing negative feedback increases gain) with C23. The front panel squelch (pin 10) or the external squelch (pin 13) apply a positive voltage from +5 to +9 VDC to CR11 or CR13. This voltage, applied to the gate of Q8, causes Q8 to act as a variable resistor.

As the resistance between the source and the drain of Q8 is lowered, C23 reduces the amount of negative feedback applied to U4B, pin 2, causing U4B gain to increase. Voltage divider R27 and CR16 assures that the source voltage will be greater than the pinch off voltage of Q8. This assures that Q8 will be cut off with no input to its gate. CR14, R35, CR15 and R37 force the emitter of Q9 to greater than +5 VDC when the squelch controls are maximum counterclockwise. This action assures that the audio gate will be open for any signal condition when the squelch control is fully counterclockwise. It should be noted that the feedback network for U4B is frequency selective (R31 and C25) and the amplifier has maximum gain at approximately 300 Hz.

The output of U4B (pin 1) is rectified in voltage doubler C44, C9 and CR10. This DC is applied between the emitter and base of Q9, causing current to flow through R35. This voltage is applied to pin 13 of U2, causing the gate to open audio to be present on pin 3. The squelch time constant is determined by C28 and R35. R50 and CR18 act as a clamp to limit the excursion of the emitter of Q9 and thereby decrease the decay time of the squelch voltage. The N.B. ON input on pin 28 (+9 volts) forces the squelch gate to be open anytime the noise blanker is on.

5.14.2.5 Audio Squelch Gate and Output Amplifier

U1D accepts the output from the product detector and drives the audio gate, U2. The audio gate can be

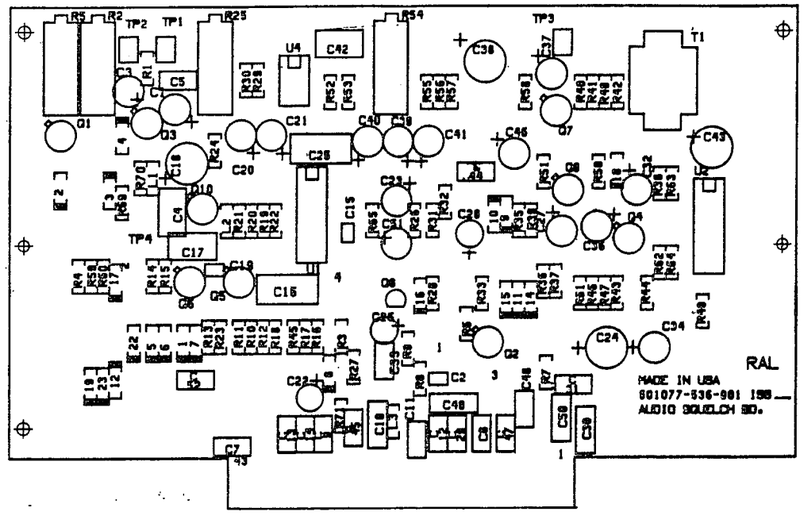
controlled by the squelch or the audio mute line, pin 32. The gated audio passes through C46, R38, pin 1 of U2, through SWA, out on pin 2 of U2 and into SWB on pin 3. The output of SWB, pin 4, drives the base of Q4 through C32. SWA or SWB of U2 can be closed to kill the speaker audio output. A logic 0 on the mute line will cause pin 5 of U2 to decrease to below +4 VDC and the audio will be killed. The mute line is used to kill the audio any time the synthesizer looses lock (for example: when changing bands). Audio amplifier Q4 can also be driven from the side tone input on pin 27. The side tone input comes from an external source from the rear panel or from the FM board 1A1A6 with that option installed.

5.14.2.6 Miscellaneous Circuitry

Q5 is the transmit switch and is energized when a logic 0 is placed on pin 15. When Q5 is turned on, +9 volts is applied to most circuitry on the board. Note that Q4 is active in transmit as well as receive because of the side tone requirement. Q6 is a DC switch and is turned on in LSB, USB, or FSK.

5.14.2.7 AGC Time Constants

The AGC time constant is determined by C3 and R69 in AGC slow. This is modified to faster decay times in AGC-medium and AGC-fast by switching other resistors externally between pin 38 and ground.



AUDIO/SQUELCH
(601077-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1	Capacitor, 1µf, 35V	600202-314-007
C2	Capacitor, .0018µf	600268-319-002
C3	Capacitor, 22µf, 25V	600297-314-016
C4,5,7-9	Capacitor, .1µf, 50V	600226-314-008
11-14,29,		
31,33,45,		
48,52		
C10,30,49,	Capacitor, .001µf	600189-314-014
50		
C15,19	Capacitor, .01µf	600268-314-008
C16,25	Capacitor, 470pf	647003-306-501
C17	Capacitor, 6.2pf	662081-308-501
C18,24,38,	Capacitor, 100µf, 25V	600297-314-032
43		
C20,23,32,	Capacitor, 4.7µf, 50V	600297-314-010
34,39,51		
C21,26,28,	Capacitor, 10µf, 50V.	600297-314-013
37,41		
C22,36,40,53	Capacitor, 1µf, 50V	600297-314-003
C27	Capacitor, 4.7µf, 10V	600202-314-014
C42	Capacitor, 24pf	624094-306-501
C46	Capacitor, 6.8µf, 50V	600297-314-012
C44	Capacitor, .1µf,, mono	600226-314-014

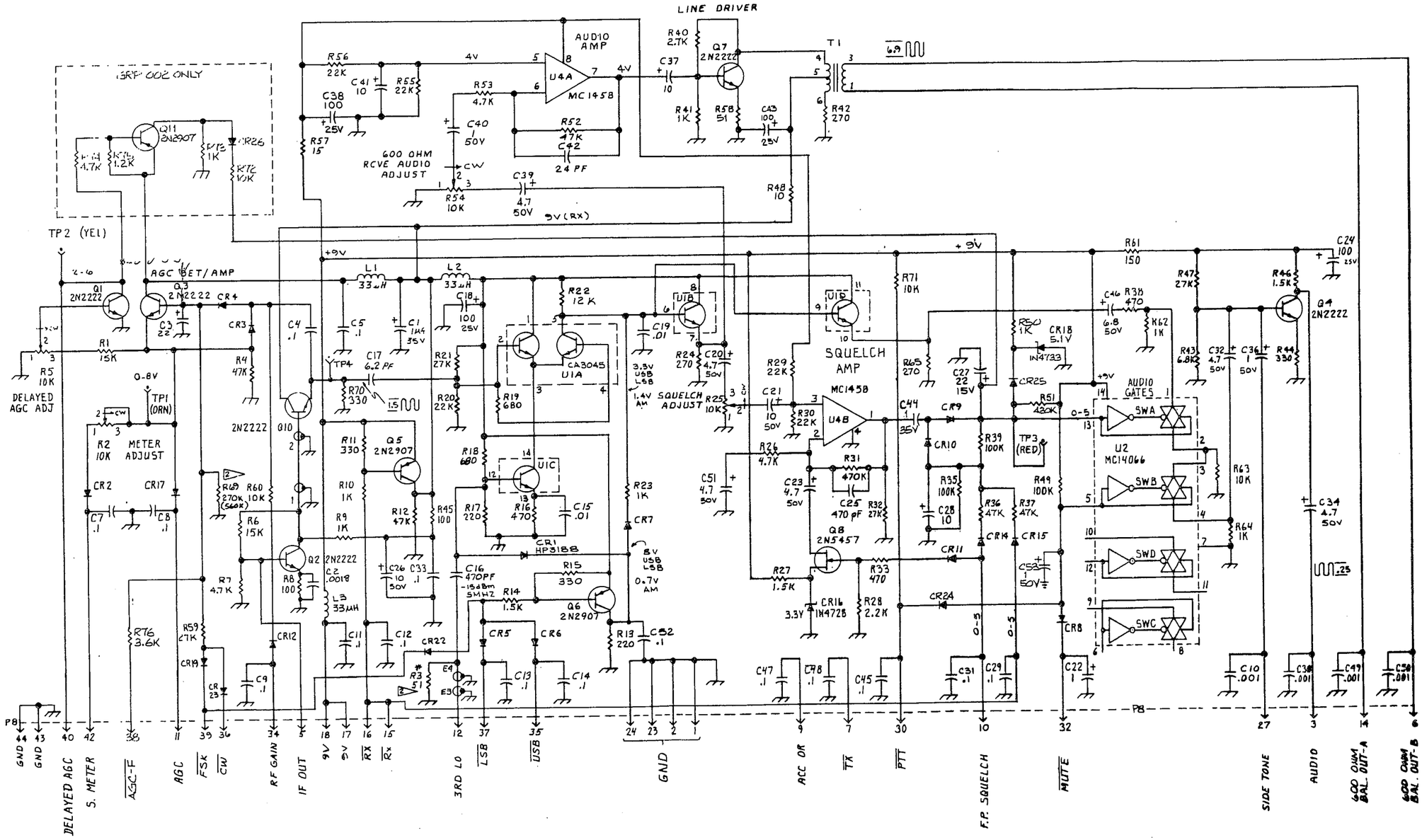
AUDIO/SQUELCH
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
CR1	Diode, HP3188	600144-410-001
CR2-12,14,	Diode, 1N4148	600109-410-001
15,17,19		
22-25		
CR16	Diode, 1N4728A	600006-411-001
CR18	Diode, 1N4733	600006-411-006
CR24,25	Diode, 1N4148	600109-410-001
CR26	Diode, 1N4148	600109-410-001
L1,2,3	Choke, 33µH	600125-376-007
R1,6	Resistor, 15K, 1/4W, 5%	615024-341-075
R2,5,25,54	Resistor, 10K, variable	600063-360-010
R3,58	Resistor, 51Ω, 1/4W, 5%	651094-341-075
R4,12,36,	Resistor, 47K, 1/4W, 5%	647024-341-075
37,52		
R7,26,53	Resistor, 4.7K, 1/4W, 5%	647014-341-075
R8,45	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R9,10,23,	Resistor, 1K, 1/4W, 5%	610014-341-075
50,62,64,		
41		
R11,15,44,	Resistor, 330Ω	633004-341-075
70		
R13,17	Resistor, 220Ω, 1/4W, 5%	622004-341-075
R14,27,46	Resistor, 1.5K, 1/4W, 5%	615014-341-075
R18,19	Resistor, 680Ω, 1/4W, 5%	668004-341-075

AUDIO/SQUELCH
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
R20,29,30,	Resistor, 22K, 1/4W, 5%	622024-341-075
55,56		
R21,32	Resistor, 27K, 1/4W, 5%	627024-341-075
R22	Resistor, 12K, 1/4W, 5%	612024-341-075
R24,42,65	Resistor, 270Ω, 1/4W, 5%	627004-341-075
R28	Resistor, 2.2K, 1/4W, 5%	622014-341-075
R31	Resistor, 470K, 1/4W, 5%	647034-341-075
R33,38,16	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R35,39,49	Resistor, 100K, 1/4W, 5%	610034-341-075
R40	Resistor, 2.7K, 1/4W, 5%	627014-341-075
R43	Resistor, 6.8K, 1/4W, 5%	668014-341-075
R47,59	Resistor, 2.7K, 1/4W, 5%	627014-341-075
R48	Resistor, 10Ω, 1/4W, 5%	610094-341-075
R51	Resistor, 430K, 1/4W, 5%	643034-341-075
R57	Resistor, 15Ω, 1/4W, 5%	615094-341-075
R58	Resistor, 51Ω, 1/4W, 5%	651094-341-075
R60,63,71	Resistor, 1K, 1/4W, 5%	610014-341-075
R61	Resistor, 150Ω, 1/4W, 5%	615004-341-075
R69	Resistor, 270K, 1/4W, 5%	627034-341-075
R72	Resistor, 10K, 1/4W, 5%	610024-341-075
R73	Resistor, 1K, 1/4W, 5%	610014-341-075
R74	Resistor, 4.7K, 1/4W, 5%	647014-341-075
R76	Resistor, 3.6K, 1/4W, 5%	636014-341-075
T1	Transformer	635234-501-001
U1	IC, CA3045	600038-415-001
U2	IC, 4066BDC	600186-415-001
U4	IC, CA1458	600039-415-001

Figure 5.20 Audio/Squelch Board Assembly



NOTES:
1. UNLESS OTHERWISE NOTED.
   RESISTORS ARE IN OHMS, 1/4 W, ±5%
   CAPACITORS ARE IN MFD
   DIODES ARE IN4148

[2] (VALUE FOR GROUP-003), * OMITTED GRP-003.

Figure 5.21 Audio/Squelch Board Schematic

AUDIO/SQUELCH BOARD

1A1A10

PIN CONNECTIONS/VOLTAGE READINGS

1A1A10-J10

(MULTI-USE BOARD: (XXXX) = PIN ASSIGMENT IN THIS APPLICATION;
N.C. = NO CONNECTIONS)

GND	1	GND
.3-3 kHz 0-0.15 VRMS AUDIO	3	
5 MHz -29 dBm IF IN	5	600 OHM REC. AUDIO OUT 0-2.4 VRMS
(N.C.) LOGIC "0" OR 1 $\overline{TX}$	7	
(N.C.) 0-+6 VDC (A3A) ACC "OR"	9	F.P. SQUELCH 0-+9 VDC
0-+6 VDC AGC (R)	11	3RD LO IN -15 dBm 5 MHz
(N.C.) 0-+9 VDC EXT. SQUELCH*	13	600 OHM REC. AUDIO OUT 0-2.4 VRMS
(GND) LOGIC "0" OR 1 $\overline{RX}$	15	$\overline{RX}$ LOGIC "0" OR 1 (GND)
+9 VDC	17	+9 VDC
	19	
	21	
GND	23	GND
	25	
1 kHz .05-2.0 VRMS SIDETONE	27	N.B. ON LOGIC "0" OR 1 (N.C.)
	29	$\overline{PTT}$ LOGIC "0" OR 1 (N.C.)
	31	$\overline{MUTE}$ LOGIC "0" OR 1
	33	"RF" GAIN 0-+9 VDC
LOGIC "0" OR 1 $\overline{USB}$	35	$\overline{CW}$ LOGIC "0" OR 1
LOGIC "0" OR 1 $\overline{LSB}$	37	DELAYED AGC +2-+6 VDC (R)
LOGIC "0" OR 1 $\overline{FSK}$	39	
	41	"S" MTR 0-+6 VDC (R) (N.C.)
GND	43	GND

BOTTOM VIEW

5.15 SPEAKER AMPLIFIER BOARD, 1A1A34

The Speaker Amplifier U1 is a monolithic audio amplifier in non-inverting configuration. R1 sets the voltage gain at 37 dB. C3, 4, 6 and R4 are compensating elements. C5 is a bootstrap capacitor which allows the output to drive close to the supply voltage. The output, pin 12, is internally biased at half the supply voltage. The circuit is normally driven from the tap of a 10K potentiometer and drives a 3.2-ohm output speaker.

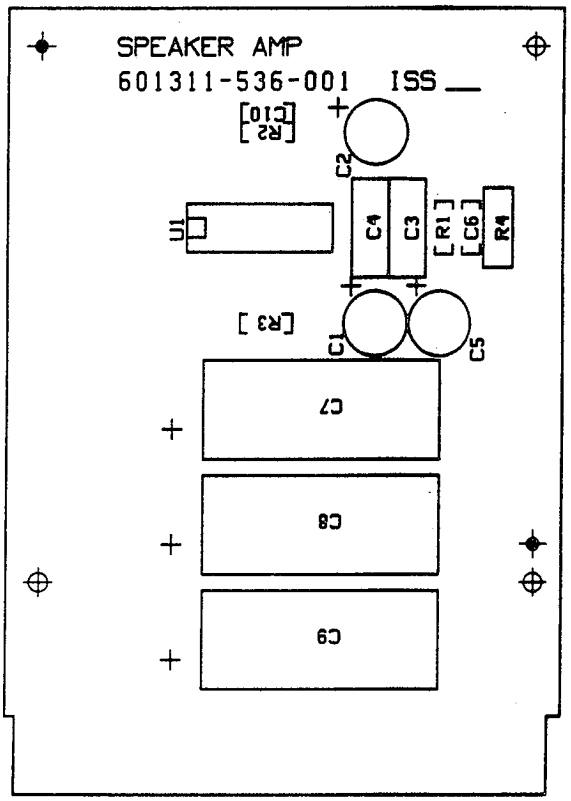
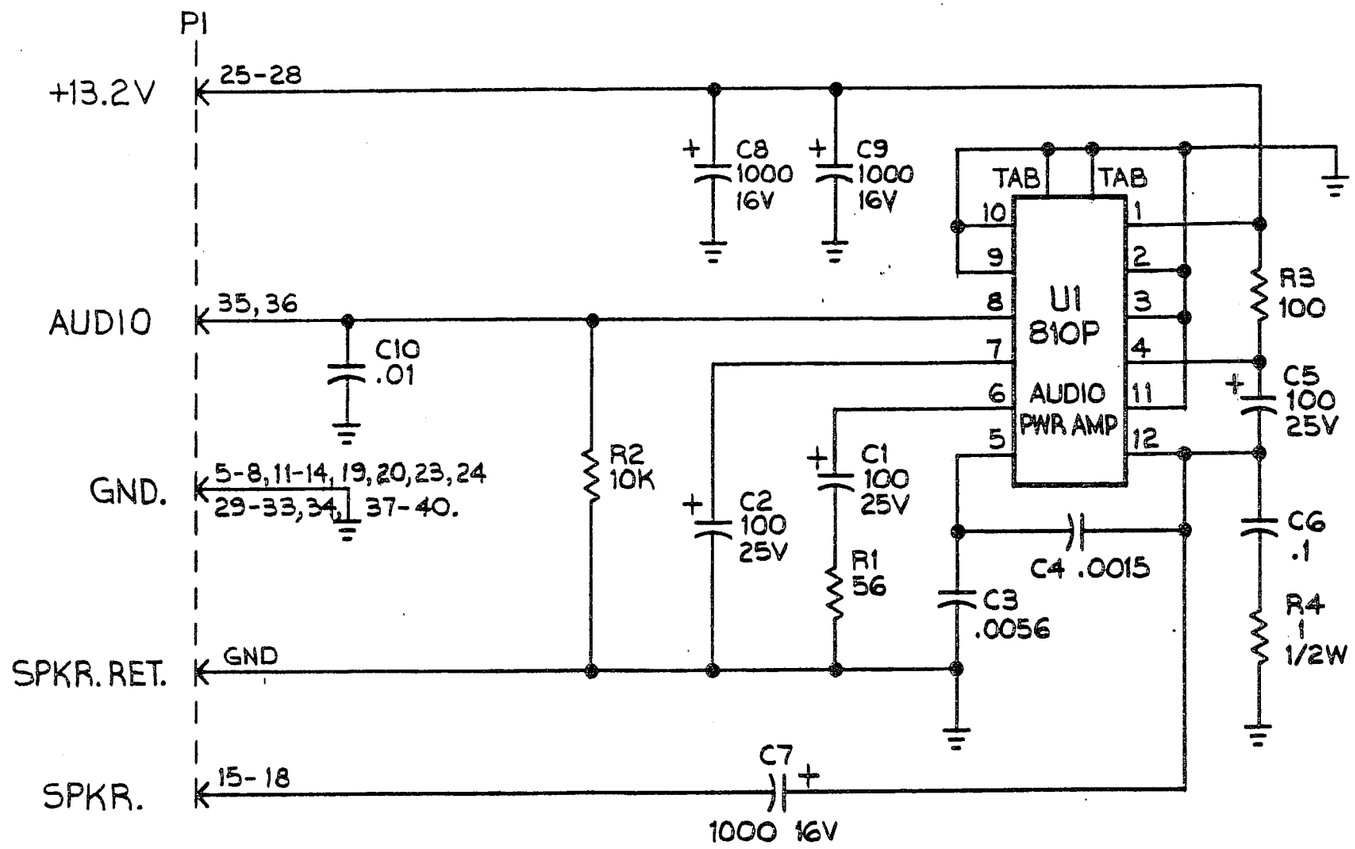


Figure 5.22 Speaker Amplifier Assembly

SPEAKER AMP
(601311-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1,2,5	Capacitor, 100µf, 25V	600297-314-032
C3	Capacitor, .0056µf, 400V	600204-314-045
C4	Capacitor, .0015µf, 400V	600204-314-040
C6	Capacitor, .1µF, 50V	600272-314-001
C7,8,9	Capacitor, 1000µf, 16V	600259-314-108
C10	Capacitor, .01µf, 50V	600272-314-003
R1	Resistor, 56Ω, 1/4W, 5%	656094-341-075
R2	Resistor, 10K, 1/4W, 5%	610024-341-075
R3	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R4	Resistor, 1.0K, 1/2W, 5%	610084-341-205
U1	IC, 810P	600216-415-001
(U1)	Heatsink	600184-419-001



NOTES

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS RATED IN OHMS, 1/4W, 5% AND ALL CAPACITORS RATED IN MFD.

Figure 5.23 Speaker Amplifier Schematic

5.16 SYNTHESIZER BOARDS

This section electrically groups the synthesizer boards which produce the three local oscillator signals for frequency translation. Included are the Reference Board 1A1A9, the Minor Loop Board 1A1A11, the Translator Loop Board 1A1A13, the Major Loop Board 1A1A15. The third LO is normally a fixed 5 MHz signal from the Reference Board. With the BFO option, the third LO is obtained from the optional BFO board. Figure 5.27 is a block diagram showing the interconnections and major functions within the boards.

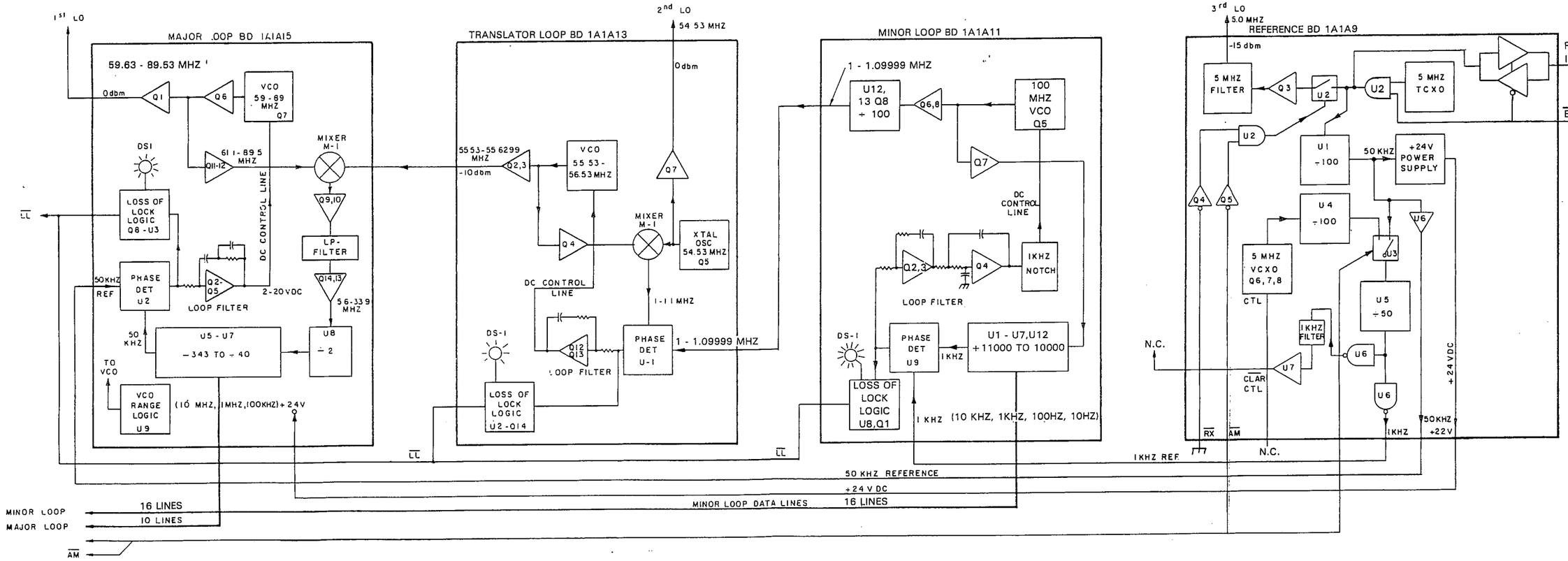


Figure 5.24 Synthesizer Block Diagram

5.16.1 REFERENCE BOARD, 1A1A9

The reference board, Figures 5.28 and 5.29, contains the 5 MHz temperature compensated crystal oscillator (TCXO), from which is derived the 50 kHz reference for the major loop, the 1 kHz reference for the minor loop and the 5 MHz third LO signal. This board also contains a +24 volt bias supply for the major loop.

The TCXO output at 5 MHz is buffered by a NAND gate (U2, pin 8). An external reference input (U2, pin 9) is available for possible future uses of this board where the reference oscillator might be mounted remotely. From U2, pin 8, the 5 MHz splits into two paths. One goes to the third LO switch, pin 1 of U2. The other goes to U1, a dual decade counter, which is connected to divide-by-100. The output of U1 on pin 3 is buffered by U6, pin 8, to become the 50 kHz reference signal to the major loop board. The 50 kHz signal also drives the voltage multiplier from U6, pin 11. Transistors Q1 and Q2 are high current drivers which drive the voltage multiplier with a 50 kHz square wave of approximately 11.5 volts peak-to-peak amplitude. Diodes CR2 through CR6 and associated capacitors form a voltage multiplier. The output is regulated to +24 volts at TP1 by zener CR1, and is designed to supply approximately 2 mA to the major loop board.

The AM and RX lines are buffered and inverted by Q4, Q5 and associated circuitry, and routed to pins 4 and 5 of U2. If the receiver is in AM, the AM line will be low, so pin of U2 will be high. This drives pin 6 (U2) low which makes pin 3 high, inhibiting the third LO output. Transistor Q3 is an emitter-follower which drives the third LO output through a harmonic filter made up of L12, L6, L7, L11 and associated capacitors. The third LO output level is adjustable with R9. The output level is normally set to 0 dBm (.224 volts RMS).

The clarifier circuit, not used in the MSR 5050, shifts the receive frequency by substituting a variable 1 kHz reference for the fixed 1 kHz, which normally supplies the minor loop. The clarifier oscillator, Q6, is a Colpitts configuration crystal oscillator whose operating frequency is determined principally by Y1, L10 and varicaps CR13 and CR12. The CLARIFIER control on the front panel varies the bias on the varicaps from 0 volts to +9 volts. This causes the frequency of the nominally 5 MHz oscillator to shift at least $\pm$1250 Hz. The output is buffered by Q7, which drives U4, a dual decade counter which is connected to divide by 100 and gives a 50 kHz output at pin 9. The clarifier will be ON only if the RX line is low and the CLRS (clarifier switch) line is low. If this is true, U2 pins 13 and 12 will be high, pin 11 will be low. This disables the pin 11 gate of U3 and enables the pin 6 gate of U3. Since pin 3 is high, Q8 is turned on, which enables the clarifier oscillator. The 50 kHz at U3, pin 8, is now being supplied by the clarifier oscillator rather than the TCXO. U5 is connected to divide by 50 to produce 1 kHz at its output, pin 3. When the clarifier is on, the 1 kHz at TP3 will vary at least $\pm$0.25 Hz with the clarifier control setting. The 1 kHz reference signal to the minor loop is provided by U6, pin 6. U6, pin 2, drives a three section RC filter which converts the square wave at pin 3 into a sine wave at R25. The lower amplifier of U7 is simply a voltage follower used

to bias the upper half output at one half of the supply voltage. Pin 1 of U7 provides the 1 kHz tone output. Additional filtering of the signal is provided by C31 and R24.

The frequency of the TCXO Y2 can be adjusted by first removing the access screw on the cover. A small screwdriver may then be used to adjust the frequency.

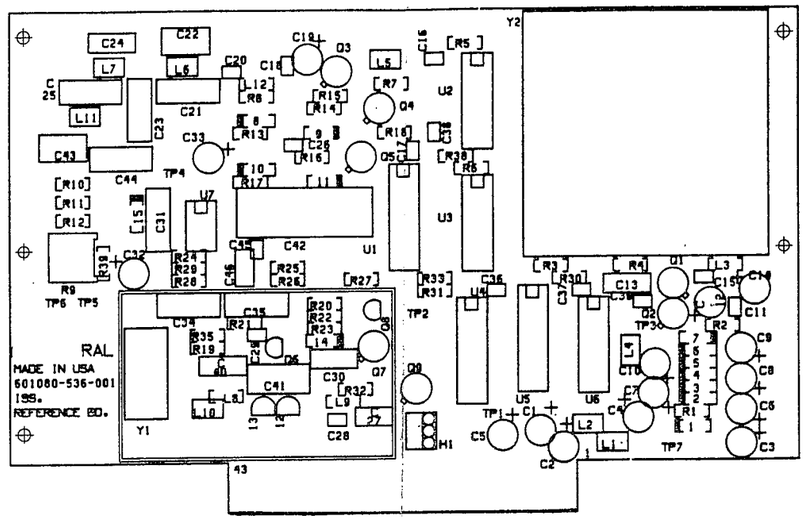


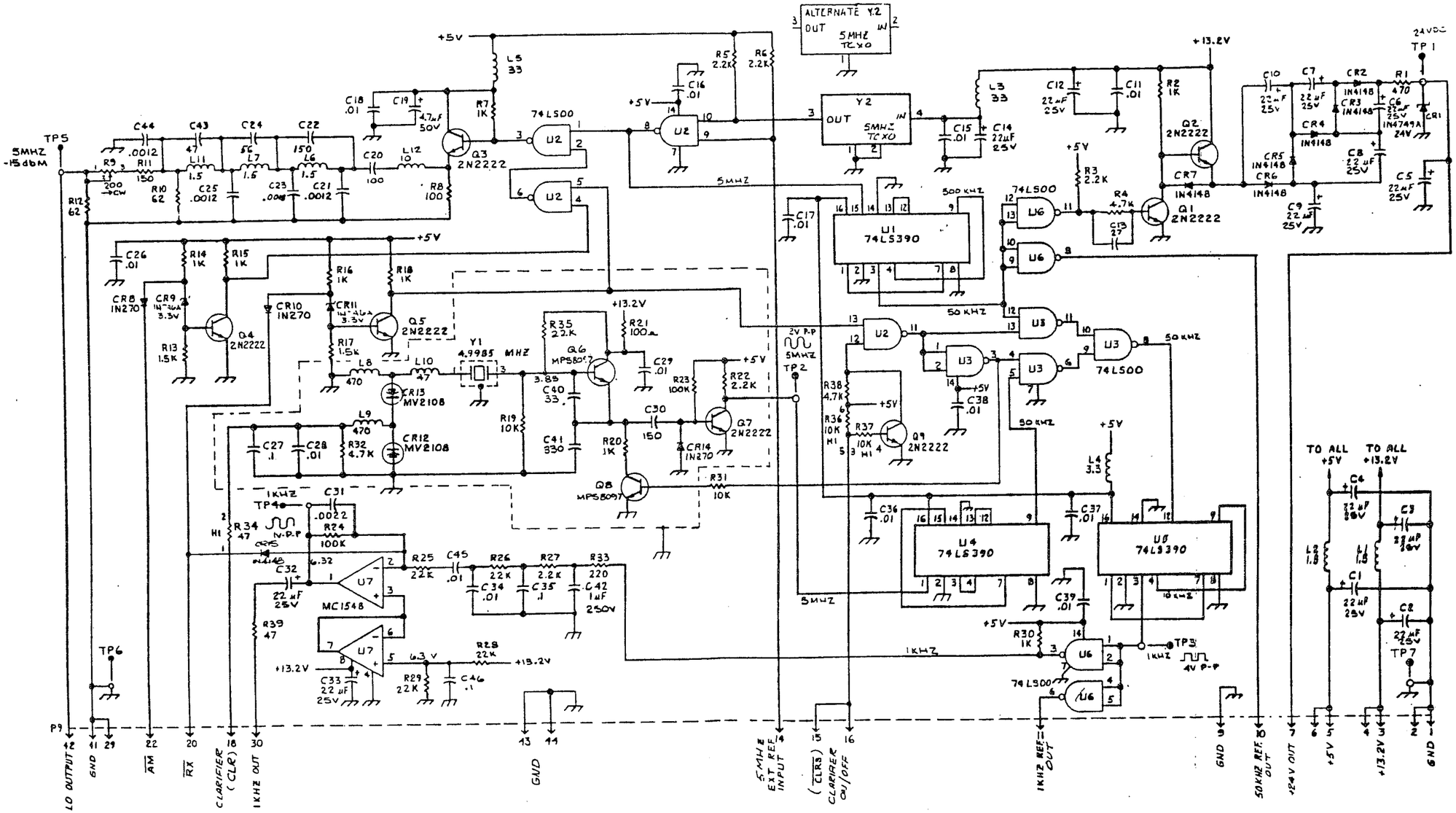
Figure 5.25 Reference Board Assembly

REFERENCE BOARD
(601080-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1-10,12, 14,32,33	Capacitor, 22µf, 25V	600297-314-016
C11,15-18, 26,28,29, 36-39,45	Capacitor, .01µf, 50V	600268-314-008
C13	Capacitor, 27pf	600269-314-016
C19	Capacitor, 4.7µf, 50V	600297-314-010
C20	Capacitor, 100pf	610003-306-501
C21,25,44	Capacitor, .0012µf	600204-314-039
C22,30	Capacitor, 150pf	615003-306-501
C23	Capacitor, .0018µf	600204-314-041
C24	Capacitor, 56pf	600269-314-024
C27,46	Capacitor, .1µf	600226-314-008
C31	Capacitor, .0022µf	600204-314-029
C34	Capacitor, .01µf	600204-314-001
C35	Capacitor, .1µf	600204-314-020
C40	Capacitor, 33pf	600269-314-018
C41	Capacitor, 330pf	633003-306-501
C42	Capacitor, 1µf, 250V	600204-314-008
C43	Capacitor, 47pf	647093-306-001
CR1	Diode, 1N4749A, 24V	600006-411-052
CR2-7,15	Diode, 1N4148	600109-410-001
CR8,10,14	Diode, 1N270	600052-410-001
CR9,11	Diode, 1N746A, 3.3V	600002-411-001
CR12,13	Diode, MV2108	600123-410-005
L1,2,6,7, 11	Choke, 1.5µH	600125-376-033
L3,5	Choke, 33µH	600125-376-007
L4	Choke, 3.3µH	600125-376-006
L8,9	Choke, 470µH	600125-376-015
L10	Choke, 47µH	600072-376-033
L12	Choke, 10µH	600125-376-032

REFERENCE BOARD
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
Q1-5,7,9	Transistor, 2N2222A	600080-413-001
Q6,8	Transistor, MPS8097	600278-413-001
R1	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R2,7,14, 15,16,18, 20,30	Resistor, 1K	610014-341-075
R3,5,6, 22,27	Resistor, 2.2K	622014-341-075
R4,32,38	Resistor, 4.7K	647014-341-075
R8,21	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R9	Resistor, 200Ω, variable	600072-360-005
R10,12	Resistor, 62Ω, 1/4W, 5%	662094-341-075
R11	Resistor, 150Ω	615004-341-075
R13,17	Resistor, 1.5K, 1/4W, 5%	615014-341-075
R19,31,36, 37	Resistor, 10K	610024-341-075
R23,24	Resistor, 100K	610034-341-075
R25,26,28 29,35	Resistor, 22K	622024-341-075
R33	Resistor, 220Ω	622004-341-075
R34,39	Resistor, 47Ω, 1/4W, 5%	647094-341-075
TP1-7	Terminal	600261-230-001
	Board marking	601080-536-903
	Screw, Ph#2-56 x 3/16	690256-203-035
	Washer, Int. TL#2	622002-217-005
U1,4,5	IC, 74L5390	600535-415-001
U2,3,6	IC, 74L500	600114-415-001
U7	IC, MC1458	600039-415-002
Y1	Crystal, 4.99850 MHz	600123-378-002
Y2	Crystal, 5 MHz	600167-378-001



NOTES:

1. UNLESS OTHERWISE NOTED.
   RESISTORS ARE IN OHMS, 1/4 W, ±5%; CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS (pF), VALUES LESS THAN ONE ARE IN MICROFARADS (μF); INDUCTORS ARE IN MICROHENRYS (μH).

Figure 5.26 Reference Board Schematic

REFERENCE BOARD

1A1A9

PIN CONNECTIONS/VOLTAGE READINGS

1A1A9-J9

	GND	1	2	GND
	+13 VDC	3	4	+13.2 VDC
	+5 VDC	5	6	+5 VDC
	+24V (±2V)	7	8	
	GND	9	10	50 kHz REF.
(N.C.)	1 kHz REF. (W/CLARI.,±25 kHz)	11	12	REF. IN/OUT
		13	14	$\overline{\text{EXT}}$
	(N.C.) $\overline{\text{CLRS}}$	15	16	$\overline{\text{CLRS}}$ (N.C.)
		17	18	CLR (N.C.)
		19	20	$\overline{\text{RX}}$ (GND)
		21	22	$\overline{\text{AM}}$ LOGIC 1 OR 0
		23	24	
		25	26	
		27	28	
	GND	29	30	1 kHz OUT
		31	32	
		33	34	
		35	36	
		37	38	
		39	40	
	GND	41	42	5 MHz-15 dBm (3RD LO)
	GND	43	44	GND

BOTTOM VIEW

5.16.2 MINOR LOOP BOARD, 1A1A11

The Minor Loop generates the small (10 Hz) steps in the synthesizer. Its output, a 1.000 to 1,09999 MHz signal, is the reference for the Translator Loop.

The VCO (Q5, C1, C2, L1 and CR1) is a Colpitts oscillator whose frequency (100.000 to 100.999 MHz) is determined by the DC voltage at the junction of CR1 and C1. The VCO output drives two isolation buffers. The first (Q6 and associated components) drives a divide by 10 prescaler U12, whose out drives U13, a divide by 10 counter. The Minor Loop output (pin 12 of U13) is passed through a filter and then applied to Q8. The second buffer (Q7 and associated components) drives U11 which drives programmable divider U1 through U6.

The programmable divider functions in the following manner: U3, U4, U5, and U6 are parallel -loadable UP/DOWN counters which are cascaded and permanently connected to count DOWN. Counter U6 is the most significant digit and is permanently connected to load 10 each time its load line goes low; U1 is the least significant. U7 is an array of open collector inverters which have their outputs connected together to form a NOR gate. The output (pins 2, 4, 6, 8, 10 and 12) can only go high if all the inputs (pins 1, 3, 5, 9, 11 and 13) are low. The U7 inputs are connected so that the output goes high when the counter (U6-U3) contains the number 002. To understand the operation, assume that the counter has just been loaded with the number 1240. The counters begin counting down.

Because the D input (pin 2) is low, pin 5 of U2 (Q) stays low and pin 6 (Q) stays high. After 10,000 pulses, U6 underflows and pin 1 (U7) goes low.

After another 100 pulses, U5 underflows and U7 (pin 3) goes low. After another 20 pulses, U4 underflows and U7 (pin 5) goes low. After another 2 pulses, pins 9, 11 and 13 of U7 are low -so the "output" of number 0020 and the D input (pin 2 of U2) goes high again loading U1, U3, U4, U5 and U6 with the divide number. The next pulse (number 000) toggles pin 6 high and pin 5 low. The cycle can now repeat. U1 controls the least significant number; when it underflows, it gets U2 (pin 9) which sets U11 to divide by 10 or 11.

The output of the programmable divider (U2, pin 5) is fed to the phase/frequency detector U9, where it is compared with the 1 kHz reference. If the divider output is too low in frequency (lagging the 1 kHz reference in phase), the phase detector output (pins 5 and 10) goes down. This causes the voltage of the VCO control line to rise, which raises the frequency to correct the error.

The loop amplifier consists of Q2 and Q3, which form a high input impedance inverting stage. The amplifier and feedback components (R20, R19, C31 and C32) form an Active Loop Filter which determines the overall loop stability. Transistor Q4 with components R17, R16, C28 and C27 forms an Active Low Pass Filter with a sharp corner and steep

roll-off to attenuate the reference sidebands.

Components R11, R10 and R12, and C24, C25 and C23 form a Twin-T Notch Filter centered on 1 kHz to further attenuate the first order sidebands.

The loss-of-lock circuitry works as follows: phase detector outputs pin 11 and pin 4 are normally high with nearly 100 percent duty cycle in a properly locked loop. This means that the base and therefore, the emitter of Q1 is also high, driving pin 2 of U8 low. This makes pins 12 and 4 of U8 high so the LED is off.

When the loop loses lock, the duty cycle will drop at either pin 11 or pin 4 (of U9). This discharges C35 through R24 faster than it can be recharged by R22 so the base voltage of Q1 drops, causing pin 2 of U8 to go high. This turns on the LED and drives the LL line low. The pin number (11 or 4) that goes low in loss-of-lock depends on whether the VCO frequency is too high or too low.

An on-card 8-volt regulator (U10) supplies the linear circuits with clean power. Table 5.5 lists the Minor Loop output frequency and divider input frequency information.

LAST 3 DIGITS OF FREQUENCY	ADJUST	DC VOLTS AT TP2
000	L9	1.98 2.22 1.58 TO 1.62
999		5.5 6.3 3.7 TO 4.9

MINOR LOOP IN LOCK VOLTAGE

Table 5.6

Minor Loop Frequency Information

FIRST 4 DIGITS OF FREQUENCY MHz	VCO FREQUENCY MHz	PROGRAM NUMBER 10 kHz	1 kHz	100 Hz	10 Hz
0000	1.00000	0	0	0	0
0001	1.00001	0	0	0	1
0002	1.00002	0	0	0	2
0003	1.00003	0	0	0	3
0004	1.00004	0	0	0	4
0005	1.00005	0	0	0	5
0006	1.00006	0	0	0	6
0007	1.00007	0	0	0	7
0008	1.00008	0	0	0	8
0009	1.00009	0	0	0	9
0010	1.00010	0	0	1	0
0020	1.00020	0	0	2	0
0030	1.00030	0	0	3	0
0040	1.00040	0	0	4	0
0050	1.00050	0	0	5	0
0060	1.00060	0	0	6	0
0070	1.00070	0	0	7	0
0080	1.00080	0	0	8	0
0090	1.00090	0	0	9	0
0100	1.00100	0	1	0	0
0200	1.00200	0	2	0	0
0300	1.00300	0	3	0	0
0400	1.00400	0	4	0	0
0500	1.00500	0	5	0	0
0600	1.00600	0	6	0	0
0700	1.00700	0	7	0	0
0800	1.00800	0	8	0	0
0900	1.00900	0	9	0	0
1000	1.01000	1	0	0	0
2000	1.02000	2	0	0	0
3000	1.03000	3	0	0	0
4000	1.04000	4	0	0	0
5000	1.05000	5	0	0	0
6000	1.06000	6	0	0	0
7000	1.07000	7	0	0	0
8000	1.08000	8	0	0	0
9000	1.09000	9	0	0	0

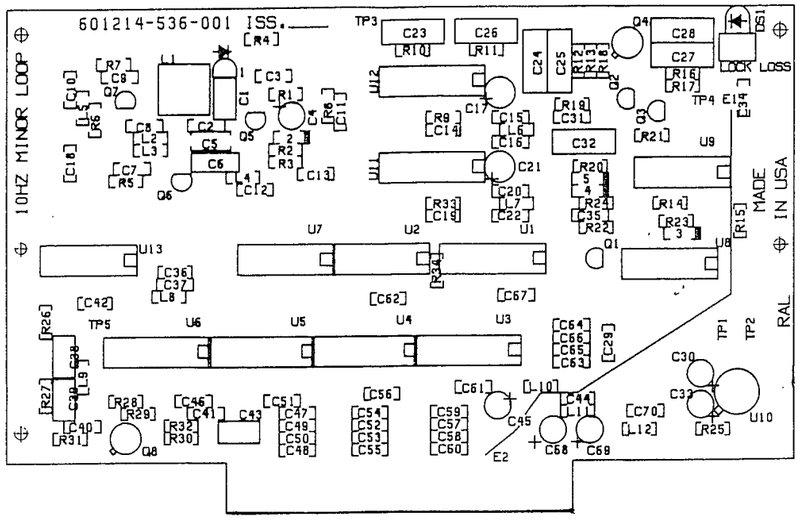


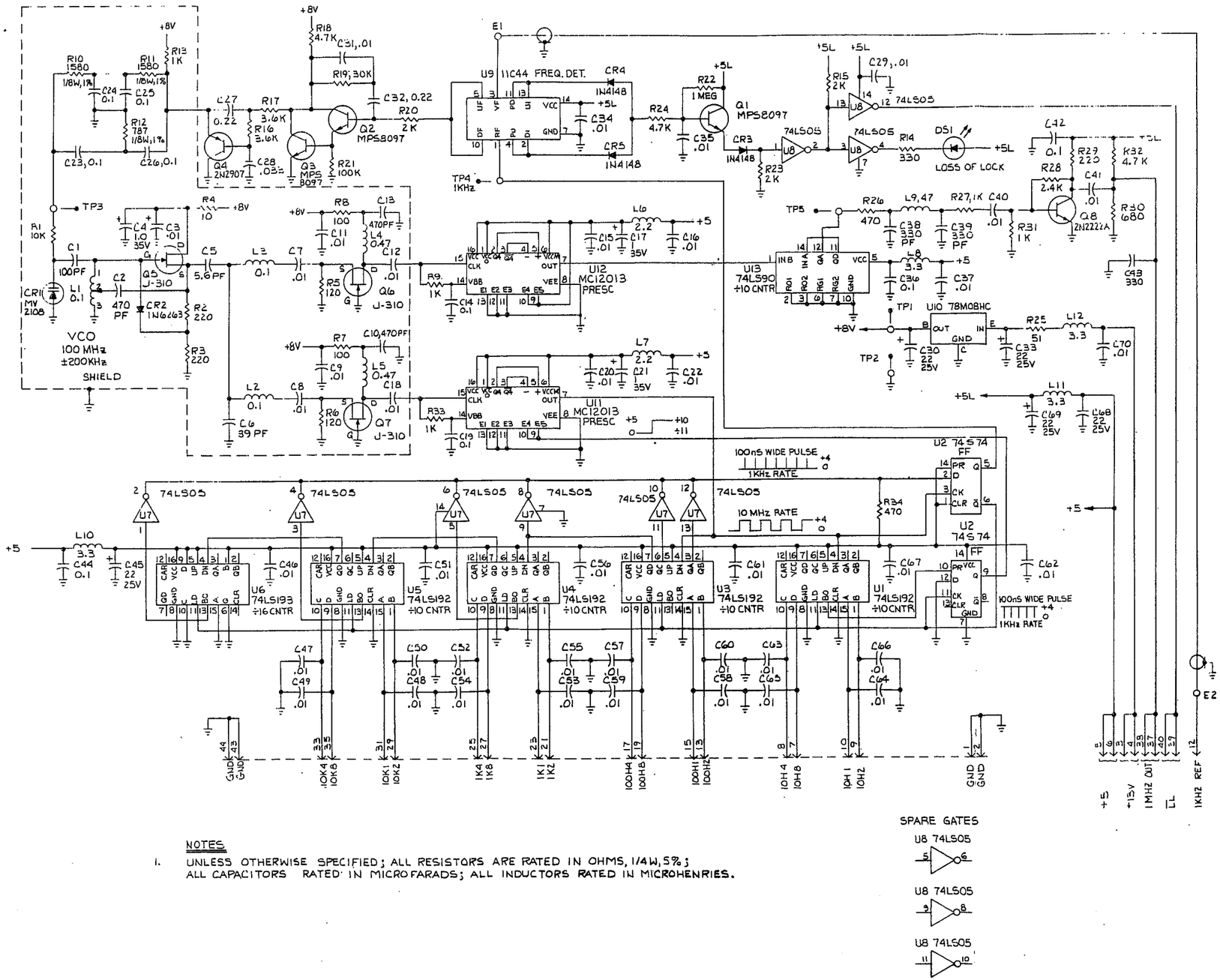
Figure 5.27 Minor Loop Board Assembly

MINOR LOOP
(601214-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1	Capacitor, 120pf, Mica	612003-306-501
C2,10,13	Capacitor, 470pf, 50V	600272-314-005
C3,7-9,11, 12,15,16, 18,20,22, 29,31,34, 35,37,40, 41,44,46- 67,70	Capacitor, .01µf, 50V	600272-314-003
C5	Capacitor, 5.6pf, NPO	600269-314-006
C6	Capacitor, 47pf, NPO	600269-314-022
C14	Capacitor, .1µf, 50V	600272-314-001
C17	Capacitor, 1.0µf, 35V	600306-314-007
C23-26	Capacitor, .1µf, MY	600204-314-020
C27,32	Capacitor, .22µf, MY	600204-314-019
C28	Capacitor, .033µf, MY	600204-314-012
C30,33,45, 68,69	Capacitor, 22µf, 25V	600297-314-016
C38,39,43	Capacitor, 330pf, Mica	633004-306-501
CR1	Diode, MV2108	600123-410-005
CR2	Diode, 1N6263	600145-410-001
CR3,4,5	Diode, 1N4148	600109-410-001
DS1	LED	600036-390-001
(DS1)	LED holder	600005-635-001
L1	Choke, .1 Var.	600173-376-001
L2,3,5	Choke, .1µH	600125-376-028
L4	Choke, .47µH	600125-376-027
L6,7	Choke, 2.2µH	600125-376-016
L8,10-12	Choke, 3.3µH	600125-376-006
L9	Choke, 47µH	600125-376-008
Q1,2,3	Transistor, MPS8097	600278-413-001
Q4	Transistor, 2N2907A	600154-413-001

MINOR LOOP
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
(Q4,8)	Transistor pad, TO-18	600025-419-001
Q5,6,7	Transistor, J310	600259-413-001
Q8	Transistor, 2N2222A	600080-413-001
R1	Resistor, 10K, 1/4W, 5%	610024-341-075
R2,3,29	Resistor, 220Ω, 1/4W, 5%	622004-341-075
R4	Resistor, 10Ω, 1/4W, 5%	610094-341-075
R5,6	Resistor, 120Ω, 1/4W, 5%	612004-341-075
R7,8	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R9,26,33,34	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R10,11	Resistor, 1580Ω, 1/8W, 1%	615811-342-059
R12	Resistor, 787Ω, 1/8W, 1%	678701-342-059
R13,27,31	Resistor, 1K, 1/4W, 5%	610014-341-075
R14	Resistor, 330Ω, 1/4W, 5%	633004-341-075
R15,20,23	Resistor, 2K, 1/4W, 5%	620014-341-075
R16,17	Resistor, 3.6K, 1/4W, 5%	636014-341-075
R18,24,32	Resistor, 4.7K, 1/4W, 5%	647014-341-075
R19	Resistor, 30K, 1/4W, 5%	630024-341-075
R21	Resistor, 100K, 1/4W, 5%	610034-341-075
R22	Resistor, 1Meg, 1/4W, 5%	610044-341-075
R25	Resistor, 51Ω, 1/4W, 5%	651094-341-075
R28	Resistor, 2.4K, 1/4W, 5%	624014-341-075
R30	Resistor, 680Ω, 1/4W, 5%	668004-341-075
TP1-5	Terminal	600261-230-001
U1,3,4,5	IC, 74LS192	600225-415-001
U2	IC, 74LS74	600113-415-001
U6	IC, 74LS193	600122-415-001
U7,8	IC, 74LS05	600240-415-001
U9	IC, 11C44	600255-415-001
U10	IC, 78M08HC	600526-415-001
(U10)	Trans. pad, TO-5	600017-419-001
U11,12	IC, MC12013	600241-415-001
U13	IC, 74LS90	600175-415-001



NOTES

1. UNLESS OTHERWISE SPECIFIED; ALL RESISTORS ARE RATED IN OHMS, 1/4W, 5%; ALL CAPACITORS RATED IN MICROFARADS; ALL INDUCTORS RATED IN MICROHENRIES.

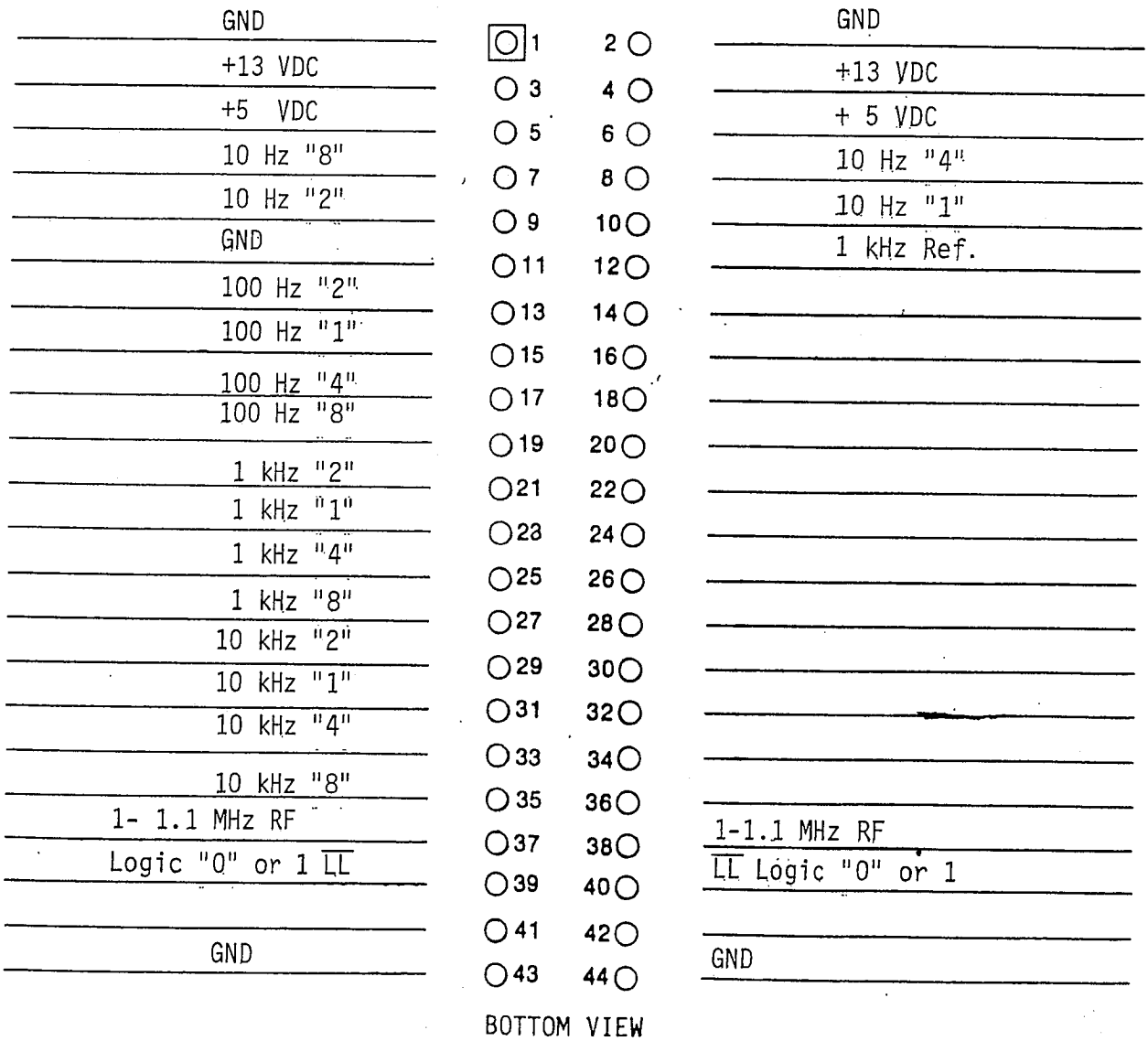
Figure 5.28 Minor Loop Board Schematic

Minor Loop Board

1A1A11

Pin Connections and Voltage Readings

1A1A11-J11



BOTTOM VIEW

5.16.3 TRANSLATOR LOOP BOARD, 1A1A13

The translator loop board, Figures 5.32 and 5.33, provides the 55.530 to 55.6299 MHz signal for use by the major loop and provides the 54.53 MHz second LO for the receiver/exciter. Also, refer to the block diagram, Figure 5.27.

The second LO signal is generated by a Colpitts configuration crystal oscillator, Q6 and associated components. The crystal is a parallel resonant type and is adjusted on frequency by trimmer C61. An uncompensated crystal can be used because both the first and second LO signals are derived from it, so any 54.53 MHz frequency drift cancels in the transmit and receive frequency, leaving the overall frequency stability dependent only on the TCXO reference oscillator.

The output of the 54.53 MHz oscillator is split into two paths. One path goes to buffer Q5, which drives mixer M1. The other path goes to buffer Q7, which provides the 0 dBm second LO output. The output amplitude can be adjusted to 0 dBm by C64. Components L13, C39, C46 and C41 form a harmonic filter.

The translator output is the sum of the second LO (54.53 MHz) and the minor loop output (1.00000 to 1.09999 MHz). The VCO, consisting of Q1, L6, C63, C60 and associated components is a Colpitts oscillator whose frequency is varied by changing the control line voltage at TP6. A change in the DC voltage here will change the bias on varicap CR4, changing the VCO tank capacitance and thus, the VCO frequency. The output signal is split into two paths. One path goes through output level adjust C15, then to cascode amplifier Q2 and Q3. The cascode amplifier provides excellent reverse isolation and a -10 dBm output level through harmonic filter L3, L2 and associated capacitors. The other path from the VCO goes to buffer Q4, which drives pin 8 of mixer M1. The output of the mixer (pins 3 and 4) is a 1.00000 to 1.09999 MHz signal. This signal is amplified by a 15 dB amplifier (Q8, Q9 and associated components) and then coupled through R54 and C57 to lowpass filter L14, L16, C54, C55 and C56 to provide a 100 millivolt p-p signal at TP4. From here, the signal is amplified by high gain common emitter amplifiers Q10 and Q11 to generate a 4 volt p-p waveform for the loop input to the phase/frequency detector (pin 1). The reference frequency is the 1.00000 to 1.09999 MHz signal from from the minor loop and is fed to pin 3 of U1. Thus, the loop translator causes the VCO to generate a frequency which, when 54.53 MHz is subtracted by M2, is the same as the minor loop input frequency.

The output of phase detector U1, is at pins 5 and 10 and is a high impedance when the loop is locked. This output is connected to a lead-lag type active loop filter consisting of Q12, Q13, R42, R41, C48, C47 and R40. The filter output goes through R43 to TP6. Diode CR7 prevents the voltage at TP6 from dropping below 4.3 volts and the VCO frequency from falling below 54.53 MHz, which would cause a false lock.

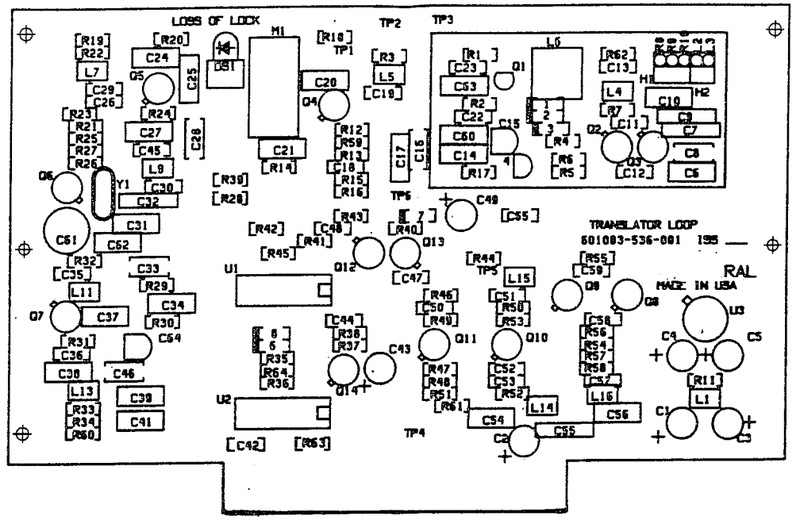
The loss-of-lock circuitry works as follows: phase detector outputs pin 11 and pin 4 are normally high with nearly 100% duty cycle in a properly locked loop. This means that the base and, therefore, the emitter of Q14 is also high, driving pin 6 of U2 low. This makes pins 8 and 10 of U2 high so the LED is off. When the loop loses lock, the duty cycle will drop at either pin 11 or pin 4 (of U1). This discharges C43 through R37 faster than it can be recharged

by R38, so the base voltage of Q14 drops causing pin 6 of U2 to go high. This turns on the LED and drives LL line low. The pin number (11 or 4) that goes low in loss-of-lock depends on whether the VCO frequency is too high or too low.

An on-card 8 volt regulator, U3, supplies the linear circuits with clean power.

LAST 3 DIGITS OF FREQUENCY	ADJUST	DC VOLTS AT TP 6
000	L6	5.6 to 5.8
999	L6	5.9 to 6.2

TRANSLATOR IN LOCK LOOP VOLTAGES



TRANSLATOR LOOP
(601083-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1-5,49	Capacitor, 22µf, 50V	600297-314-018
C6	Capacitor, 30pf	600269-314-017
C7,9	Capacitor, 82pf	600269-314-028
C8,16	Capacitor, 2.2pf	600269-314-002
C10,20,21, 24,25,37- 39,41	Capacitor, 27pf	600269-314-016
C11-13,18, 19,23,26, 29,30,35, 36,45,48, 65	Capacitor, .01µf, X7R	600272-314-003
C14	Capacitor, 68pf	600269-314-026
C15,64	Capacitor, 3-10pf, trim	600052-317-001
C17,27, C34,60,63	Capacitor, 47pf	600269-314-022
C22	Capacitor, 470pf, NPO	600272-314-005
C28,46,62	Capacitor, 10pf	600269-314-009
C31,32,33	Capacitor, 75pf	600269-314-027
C42	Capacitor, .001µf, X7R	600272-314-008
C43	Capacitor, 1µf, tant., 35V	600202-314-007
C44,50-53, C57-59	Capacitor, .1µf, 50V	600272-314-001
C47	Capacitor, .1µf, mylar	600204-314-020
C54,56	Capacitor, 130pf	600269-314-033
C55	Capacitor, 160pf	600269-314-035
C61	Capacitor, 9-35pf, trim	600018-317-004
CR4	Diode, MV2109	600123-410-008
CR6-8	Diode, 1N4148	600109-410-001
DS1	LED	600036-390-001

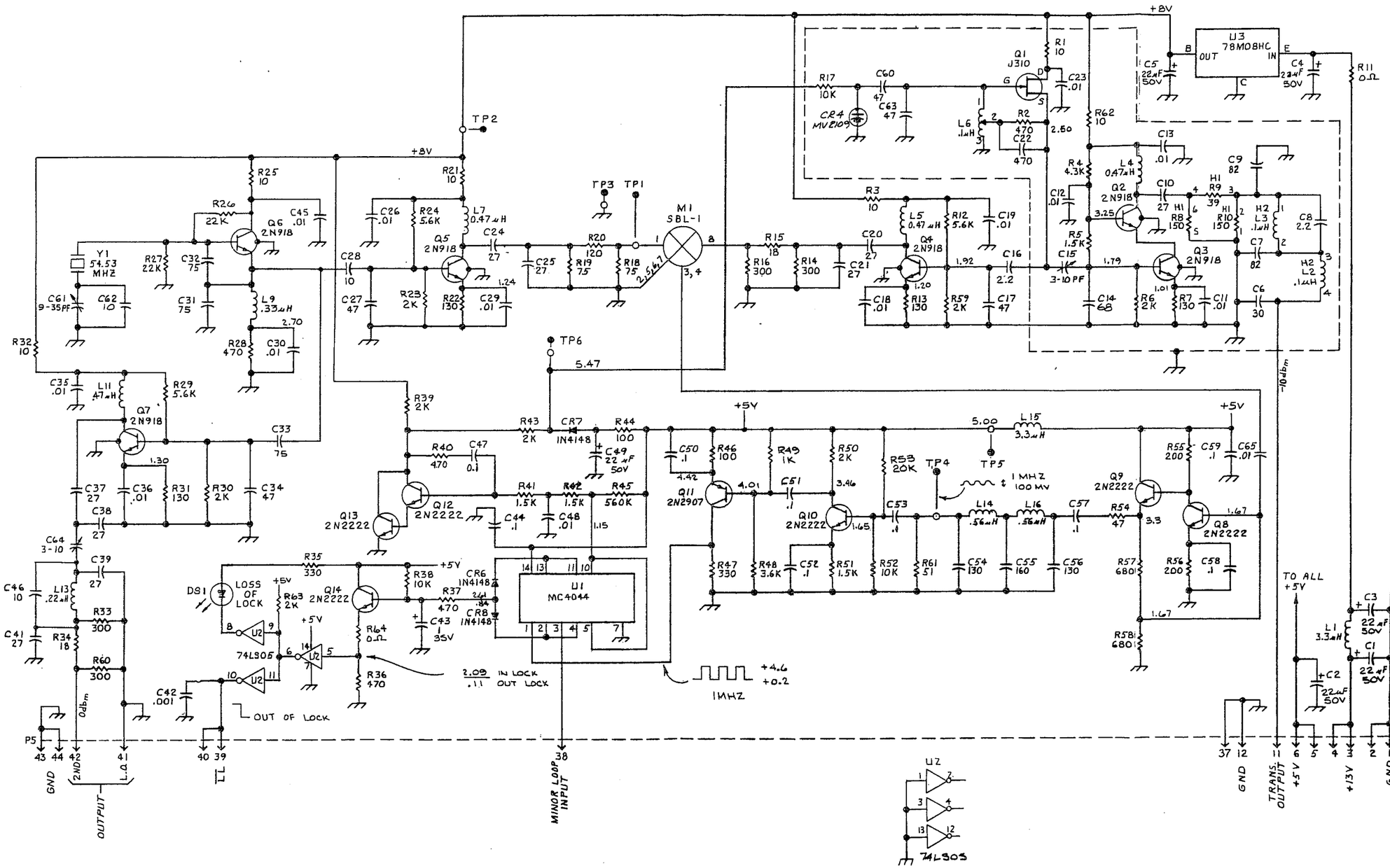
TRANSLATOR LOOP
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
H1	Vert. mount 3	600064-419-003
H2	Vert. mount 2	600064-419-004
L1,15	Choke, 3.3µH	600125-376-006
L2,3	Choke, .1µH	600125-376-028
L4,5,7, 11	Choke, .47µH	600125-376-027
L6	Choke, .1µH, variable	600173-376-001
L9	Choke, .33µH	600125-376-001
L13	Choke, .22µH	600125-376-003
L14,16	Choke, .56µH	600125-376-005
M1	Mixer	600008-455-001
Q1	Transistor, J310	600259-413-001
Q2-7	Transistor, 2N918	600085-413-001
(Q2-14)	Transistor pad	600025-419-001
Q8-10, 12-14	Transistor, 2N2222A	600080-413-001
Q11	Transistor, 2N2907A	600154-413-001
R1,3,21, 25,32,62	Resistor, 10Ω, 1/4W, 5%	610094-341-075
R2,28,36, 37,40	Resistor, 470Ω	647004-341-075
R4	Resistor, 4.3K	643014-341-075
R5,41,42 51	Resistor, 1.5K	615014-341-075
R6,23,30, 39,43,50, 59,63	Resistor, 2K	620014-341-075
R7,13,22, 31	Resistor, 130Ω	613004-341-075

TRANSLATOR LOOP
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
R8,10	Resistor, 150Ω	615004-341-075
R9	Resistor, 39Ω	639094-341-075
R11,64	Resistor, 0Ω, 1/4W, 5%	600000-341-075
R12,24,29	Resistor, 5.6K	656014-341-075
R14,16,33 R60	Resistor, 300Ω	630004-341-075
R15,34	Resistor, 18Ω	618094-341-075
R17,38,52	Resistor, 10K	610024-341-075
R18,19	Resistor, 75Ω, 1/4W, 5%	675094-341-075
R20	Resistor, 120Ω, 1/4W, 5%	612004-341-075
R26,27	Resistor, 22K	622024-341-075
R35,47	Resistor, 330Ω	633004-341-075
R44,46	Resistor, 100Ω	610004-341-075
R45	Resistor, 560K	656034-341-075
R48	Resistor, 3.6K	636014-341-075
R49	Resistor, 1K	610014-341-075
R53	Resistor, 20K	620024-341-075
R54	Resistor, 47Ω	647094-341-075
R55,56	Resistor, 200Ω	620004-341-075
R57,58	Resistor, 680Ω	668004-341-075
R61	Resistor, 51Ω, 1/4W, 5%	651094-341-075
TP1-6	Terminal	600261-230-001
U1	MC4044	600092-415-001
U2	IC, 74LS05	600240-415-001
U3	IC, 78M08HC	600526-415-001
(U3)	Trans. pad TO-5	600017-419-001
XDS1	Mount LED	600005-635-001
Y1	Crystal, 54.53 MHz	600163-378-001

Figure 5.29 Translator Loop Board Assembly



NOTES:
1. UNLESS OTHERWISE NOTED:
   RESISTORS ARE IN OHMS, 1/4W, ±5%
   CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS (pF), VALUES LESS THAN ONE ARE MICROFARADS(μF).

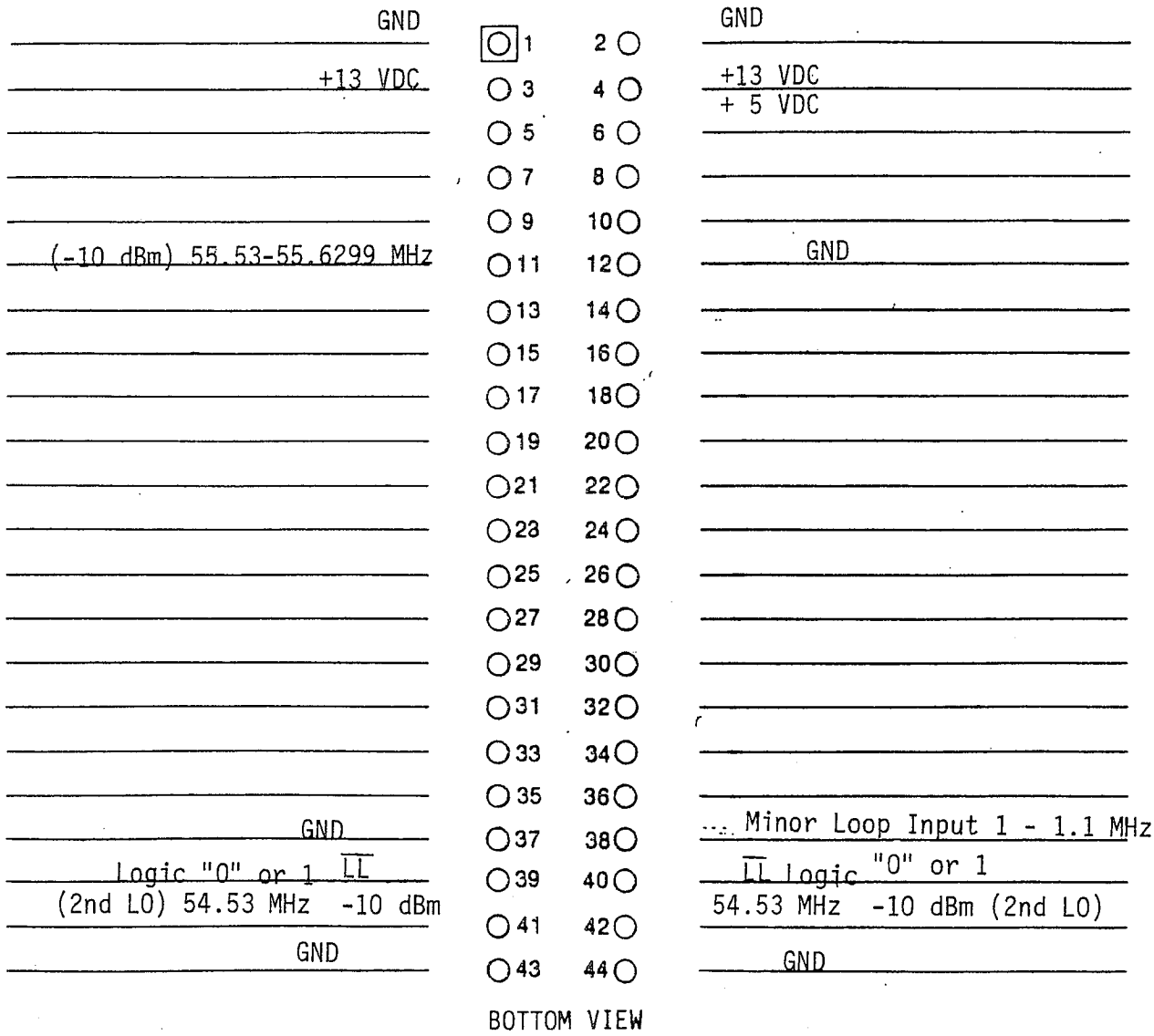
Figure 5.30 Translator Loop Board Schematic

Translator Loop Board

1A1A13

Pin Connections and Voltage Readings

1A1A13 -J13



BOTTOM VIEW

5.16.4 MAJOR LOOP BOARD, 1A1A15

The major loop, Figures 5.34 and 5.35, provides the first local oscillator (LO) signal (59.53 MHz to 89.53 MHz) for the first mixer in the signal path. The loop itself uses a 50 kHz reference frequency and generates 10 MHz, 1 MHz, and 100 kHz steps. Smaller step sizes are possible by stepping the translator RF input to the major loop from 55.53 MHz to 55.6299 MHz. The translator loop takes 10 Hz steps over this range, which also gives the major loop output 10 Hz steps. The smaller step sizes are actually generated by the minor loop, so different step sizes are possible by changing minor loops. Refer to the block diagram, Figure 5.27.

The VCO, Q7, is a Colpitts oscillator with three switched ranges. The VCO control line is the junction of varicaps CR7 and CR8 driven through decoupling choke, L4. The oscillator covers 59.53 MHz to 89.53 MHz in three course ranges (see Table 5.6). This keeps the loop gain expression $\frac{Kvkp}{N}$ * nearly constant which insures that loop dynamics (stability, settling time) are constant throughout the range. Range switching is accomplished by PIN diodes CR13 and CR2. The top range has only varicaps CR7 and CR8 in combination with L3 determining the VCO frequency. In the middle range, CR2 is turned on, which puts C71 and C73 in parallel with the varicaps. In the low range, CR2 remains on and CR13 turned on, which adds parallel capacitors C72 and C74 to the tank circuit. Diodes CR4, CR5 and CR6 limit the oscillation amplitude. Resistor R23 sets the static FET operating point an unbypassed resistor R13 degenerates the gain slightly to limit high order harmonic production.

The output of Q6 is taken from 3:1 broadband transformer L1 (L7 and L8 are similar transformers) and fed to two additional buffers. Cascode amplifiers Q12 and Q11 provide extremely good reverse isolation (70 to 80 dB) and feeds mixer M1.

The first LO output is from buffer Q1. Components L9, L10, C42, C43 and C77 provide harmonic filtering. R52 is used to adjust the output level.

The translator loop frequency is fed to pin 1 of mixer M1 and the VCO is fed to pin 8. The output, on pins 3 and 4, is amplified by Q9 and Q10 and fed to a bandpass filter consisting of L5, L6 and associated capacitors. The filter passes the difference frequency of 4 to 33.9 MHz to be further amplified by Q13 and Q14. Both the Sum F_{VCO} + FTRANS and difference F_{VCO} - FTRANS are present in the mixer output. We want only the difference frequency. The output is fed to the clock input of U8, which is a D flip-flop connected to toggle (-2). Resistors R44 and R48 bias U8's clock input at threshold for reliable triggering. The presence of the -2 is compensated for by using a 50 kHz (not 100 kHz) reference signal for the loop.

The programmable divider determines the VCO frequency in the following manner: the output of the programmable divider (U8, pin 9) is always 50 kHz if the loop is locked. The input frequency (U8, pin 11), then, is N x 50 kHz, when N is the programmed divide number. Working back up to the VCO: (N x 50 kHz x 2) + F_{TRANS} = FVCO.

The programmable divider functions in the following manner: U5, U6 and U7 are parallel - loadable UP/DOWN counters which are cascaded and permanently connected to count DOWN. Counter U5 is the most significant

digit, U7 the least significant. U4 is an array of open collector inverters which have their outputs connected together to form a NOR gate. The output (pins 4, 6, 8, 10 and 12) can only go high if all the inputs (pins 3, 5, 9, 11 and 13) are low. The U4 inputs are connected so that the output goes high when the counter (U5-U7) contains the number 002. To understand the operation, assume that the counter has just been loaded with the number 124. The counters begin counting down. Because of the D input, pin 12, is low, pin 9 of U8 (Q) stays low and pin 8 (Q) stays high. After 100 pulses, U5 underflows and U4, pin 3, goes low. After another 20 pulses, U6 underflows and U4, pin 5, goes low. After another 2 pulses, pins 9, 11 and 13 of U8 are low, so the "output" of U4, pins 4, 6, 8, 10 and 12 can go high. The counter now contains the number 002 and the D input, pin 12 of U8 goes high (this is the programmable divider output pulse), and pin goes low, again loading U5, U6 and U7 with the divide number. The next pulse (number 000) toggles pin 8 high and pin 9 low. The cycle can now repeat.

The output of the programmable divider (U8, pin 9) is fed to the phase/frequency detector U2, where it is compared with the 50 kHz reference. If the divider output is too low in frequency or lagging the 50 kHz reference in phase, the phase detector output (pins 5 and 10) goes down. This causes the voltage of the VCO control line to rise, which raises the frequency to correct the error.

The loop amplifier consists of Q5, Q4 and Q3, which form a high input impedance inverting stage. The amplifier and feedback components (C7, R12, R11 and C8 form an active loop filter, which determines the overall loop stability. Transistor Q2, with components R10, R58, C12 and C66 forms an active lowpass filter with a sharp corner and steep rolloff to attenuate the reference sidebands. The amplifier and active lowpass are fed +24 volts from the reference board. The +24 volts is needed to increase the varicap range.

The loss-of-lock circuitry works as follows: phase detector outputs pin 11 and pin 4 are normally high with nearly 100% duty cycle in a properly locked loop. This means that the base and, therefore, the emitter of Q8 is also high, driving pin 4 of U3 low. This makes pins 2 and 6 of U3 high so the LED is off. When the loop loses lock, the duty cycle will drop at either pin 11 or 4 (of U2). This discharges C25 through R32 faster than it can be recharged by R25, so the base voltage of Q8 drops causing pin 4 of U3 to go high. This turns on the LED and drives the LL line low. The pin number (11 or 4) that goes low in loss-of-lock depends on whether the VCO frequency is too high or too low.

An on-card 8 volt regualtor, U1, supplies the linear circuits with clean power.

*While a complete discussion of loop theory is beyond the scope of this technical description, the following is an extremely simplified explanation: the loop response time and setting time depends on the time constants of the loop filter components and the loop "gain" $\frac{KvKp}{N}$, where Kv is the VCO transfer constant in Radians/Sec/Volt, Kp is the phase detector constant in Volts/Radian, and N is the programmable divide number. Typical numbers for the major loop might be:

Kv = 3.14 x 106

Kp = .44 so $\frac{KvKp}{N}$ = 11.1 x 103

N = 124

Table 5.6 lists the major loop VCO output frequency and divider program information.

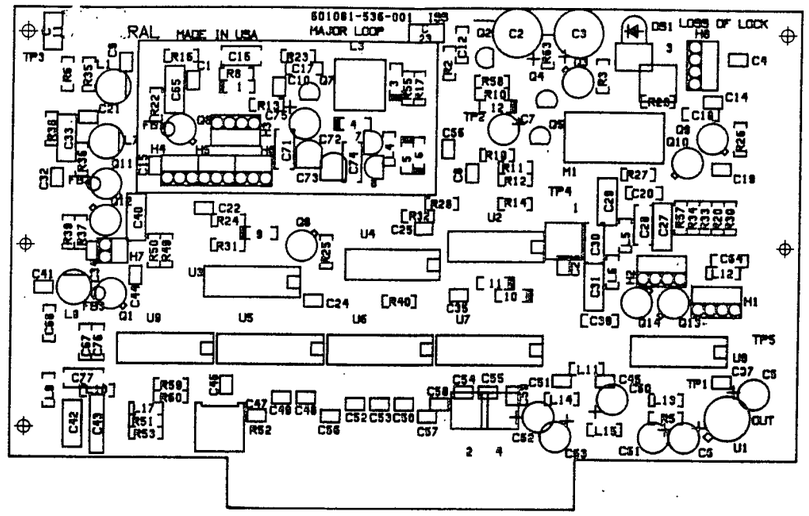
Table 5.7

Major Loop Frequency Information

FIRST 3 DIGITS OF RECEIVE FREQUENCY MHz	VCO FREQUENCY MHz	PROGRAM NUMBER	U9 PIN 8	U9 PIN 6	CR13	CR2
0.00 to 5.90	59.53 to 65.43	040 to 099	LOW	LOW	ON	ON
6.00 to 15.90	65.53 to 75.43	100 to 199	HIGH	LOW	ON	OFF
16.00 to 29.90	75.53 to 89.43	200 to 399	HIGH	HIGH	OFF	OFF

FIRST 3 DIGITS OF FREQUENCY MHZ	ADJUST	DC VOLTS TP2
29.9	L3	18.4 to 18.6
16.0		3.6 to 5.00
15.9	C72	18.2 to 18.7
06.0		2.9 to 4.5
05.9	C73	18.2 to 18.7
01.6		5.50 to 5.70

Major Loop In-Lock Loop Voltage



MAJOR LOOP
(601081-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1,4,9, 10,14,19, 21,22,24-26,32,34, 35,37,41, 44-59	Capacitor, .01µf, 50V	600268-314-008
C2,3	Capacitor, 47µf, 50V	600297-314-026
C5,6,60, 61,62,63, 75	Capacitor, 22µf, 25V	600297-314-016
C7	Capacitor, .22µf	600202-314-003
C8	Capacitor, .015µf	600268-314-011
C11,23	Capacitor, 1µf	600226-314-014
C12	Capacitor, .001µf, X7R	600272-314-008
C15	Capacitor, 100pf	600267-314-002
C16,28	Capacitor, 2.2pf, NPO	600269-314-002
C17,36,68, 69,70	Capacitor, 470pf, NPO	600272-314-005
C18,20,38, 64,67,76	Capacitor, .1µf, 50V	600272-314-001
C27,31	Capacitor, 18pf, NPO	600269-314-012
C29	Capacitor, 22pf	600269-314-014
C30	Capacitor, 1pf	600269-314-001
C33,40,65	Capacitor, 47pf	600269-314-022
C39	Capacitor, .01µf, X7R	600272-314-007
C42	Capacitor, 27pf	600269-314-016
C43	Capacitor, 75pf	600269-314-027
C66	Capacitor, .0027µf	600268-314-004
C71	Capacitor, 10pf	600269-314-009
C72,73	Capacitor, 3-10pf, variable	600052-317-001
C74	Capacitor, 6.8pf	600269-314-007
C77	Capacitor, 15pf	600269-314-011
CR1	Diode, 1N4728A, 4V	600006-411-001
CR2,13	Diode, 5022-3188	600144-410-001

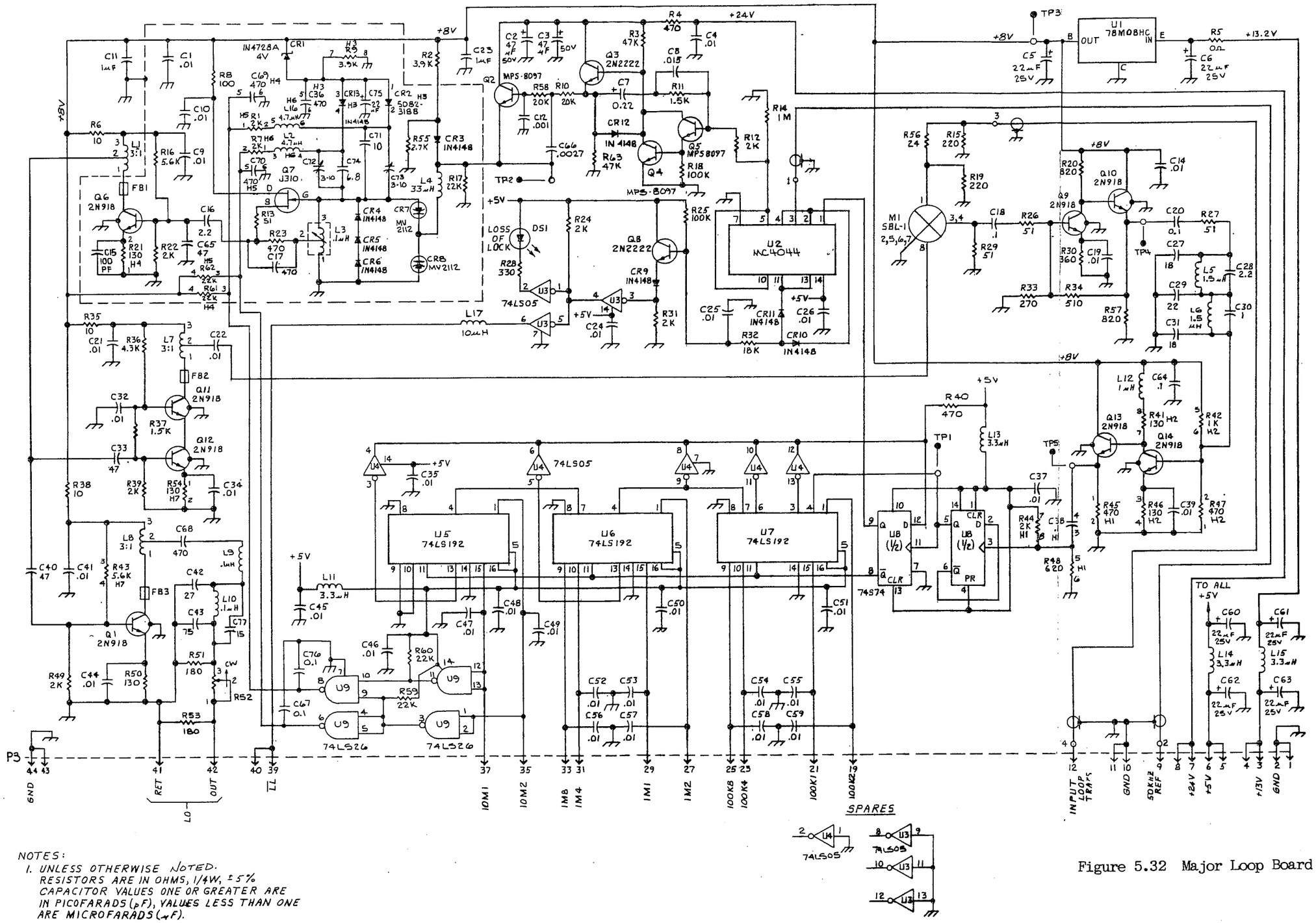
MAJOR LOOP
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
CR3-6,9-12	Diode, 1N4148	600109-410-001
CR7,8	Diode, MV2112	600123-410-009
DS1	LED	600036-390-001
H1-3,48	Vert. mount 4	600064-419-001
H4-6	Vert. mount 3	600064-419-003
H7	Vert. mount 2	600064-419-004
L1,7,8	Transformer, 3:1	600094-512-001
L2,16	Choke, 4.7µH	600125-376-030
L3	Coil, .1µH	600173-376-001
L4	Choke, 33µH	600125-376-007
L5,6	Choke, 1.5µH	600125-376-033
L9,10	Choke, .1µH	600125-376-028
L11,13-15	Choke, 3.3µH	600125-376-006
L12	Choke, 1µH	600125-376-040
L17	Choke, 10µH	600125-376-032
M1	Mixer, SLB-1	600008-455-001
Q1,6,9-14	Transistor, 2N918	600085-413-001
Q2,4,5	Transistor, MPS8097	600278-413-001
Q3,8	Transistor, 2N2222A	600080-413-001
Q7	Transistor, J310	600259-413-001
R55	Resistor, 2.7K, 1/4W, 5%	627014-341-075
R1,7,12, 22,24,31, 39,44,49	Resistor, 2K, 1/4W, 5%	620014-341-075
R2,9	Resistor, 3.9K, 1/4W, 5%	639014-341-075
R3,63	Resistor, 47K, 1/4W, 5%	647024-341-075
R42	Resistor, 1K, 1/4W, 5%	610014-341-075
R5	Resistor, 0Ω, 1/4W, 5%	600000-341-075
R6,35,38	Resistor, 10Ω, 1/4W, 5%	610094-341-075

MAJOR LOOP
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
R8	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R10,58	Resistor, 20K, 1/4W, 5%	620024-341-075
R4,23,40	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R45,47		
R13,26,27, 29	Resistor, 51Ω, 1/4W, 5%	651094-341-075
R14	Resistor, 1M, 1/4W, 5%	610044-341-075
R15,19	Resistor, 220Ω, 1/4W, 5%	622004-341-075
R16,43	Resistor, 5.6K, 1/4W, 5%	656014-341-075
R17,59-62	Resistor, 22K, 1/4W, 5%	622024-341-075
R18,25	Resistor, 100K, 1/4W, 5%	610034-341-075
R20,57	Resistor, 820Ω, 1/4W, 5%	682004-341-075
R21,41,46	Resistor, 130Ω, 1/4W, 5%	613004-341-075
50,54		
R28	Resistor, 330Ω, 1/4W, 5%	633004-341-075
R30	Resistor, 360Ω, 1/4W, 5%	636004-341-075
R32	Resistor, 18K, 1/4W, 5%	618024-341-075
R33	Resistor, 270Ω, 1/4W, 5%	627004-341-075
R36	Resistor, 4.3K, 1/4W, 5%	643014-341-075
R11,37	Resistor, 1.5K, 1/4W, 5%	615014-341-075
R48	Resistor, 620Ω, 1/4W, 5%	662004-341-075
R51,53	Resistor, 180Ω, 1/4W, 5%	618004-341-075
R34	Resistor, 510Ω, 1/4W, 5%	651004-341-075
R56	Resistor, 24Ω, 1/4W, 5%	624094-341-075
R52	Resistor, 100Ω, variable	600072-360-004
	Heatsink	600145-419-001
TP1-5	Test point	600261-230-001
U1	IC, 78M08HC	600526-415-001
U2	IC, MC4044	600092-415-001
U3,4	IC, 74LS05	600240-415-001
U5,6,7	IC, 74LS192	600225-415-001
U8	IC, 74S74	600157-415-001
U9	IC, 74LS26	600221-415-001
XDS1	Mount, LED	600005-635-001

Figure 5.31 Major Loop Board Assembly



NOTES:
1. UNLESS OTHERWISE NOTED.
   RESISTORS ARE IN OHMS, 1/4W, ±5%
   CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS (pF), VALUES LESS THAN ONE ARE MICROFARADS (μF).

Figure 5.32 Major Loop Board Schematic

MAJOR LOOP BOARD

1A1A15

Pin Connections and Voltage Readings

1A1A15-J15

GND	1	2		GND
+13 VDC	3	4		+13 VDC
	5	6		
+24 VDC	7	8		+24 VDC
50 kHz Ref.	9	10		GND
GND	11	12		55.53-55.6299 MHz -10 dBm
	13	14		
	15	16		
	17	18		
100 kHz "2"	19	20		
100 kHz "1"	21	22		
100 kHz "4"	23	24		
100 kHz "8"	25	26		
1 MHz "2"	27	28		
1 MHz "1"	29	30		
1 MHz "4"	31	32		
1 MHz "8"	33	34		
10 MHz "2"	35	36		
10 MHz "1"	37	38		
Logic "0" or 1 $\overline{LL}$	39	40		$\overline{LL}$ Logic "0" or 1
	41	42		59.63 - 89.53 MHz 0 dBm (1st LO)
GND	43	44		GND

BOTTOM VIEW

5.17 FRONT PANEL ASSEMBLY, 1A21

The front panel assembly contains all the controls and indicators for operating the receiver. Mounted to the front panel are the display board (1A21A1), keypad board (1A21A2), speaker (LS1), phone jack (J1) and controls for volume/power on (R2/S2), squelch (R3) and speaker on/off (S1).

The front panel is detachable from the receiver by 4 nuts, 3 screws and 4 ribbon cable connectors. The following sections describe the attached keypad and display boards which contain the majority of electrical connections to the receiver via three ribbon cable connectors: two from the display board (P1, P2) and one from the keypad board (P1). The connections to the receiver are made to the interface board (1A1) which in turn connects to the mother board by its 88 pin edge card connector.

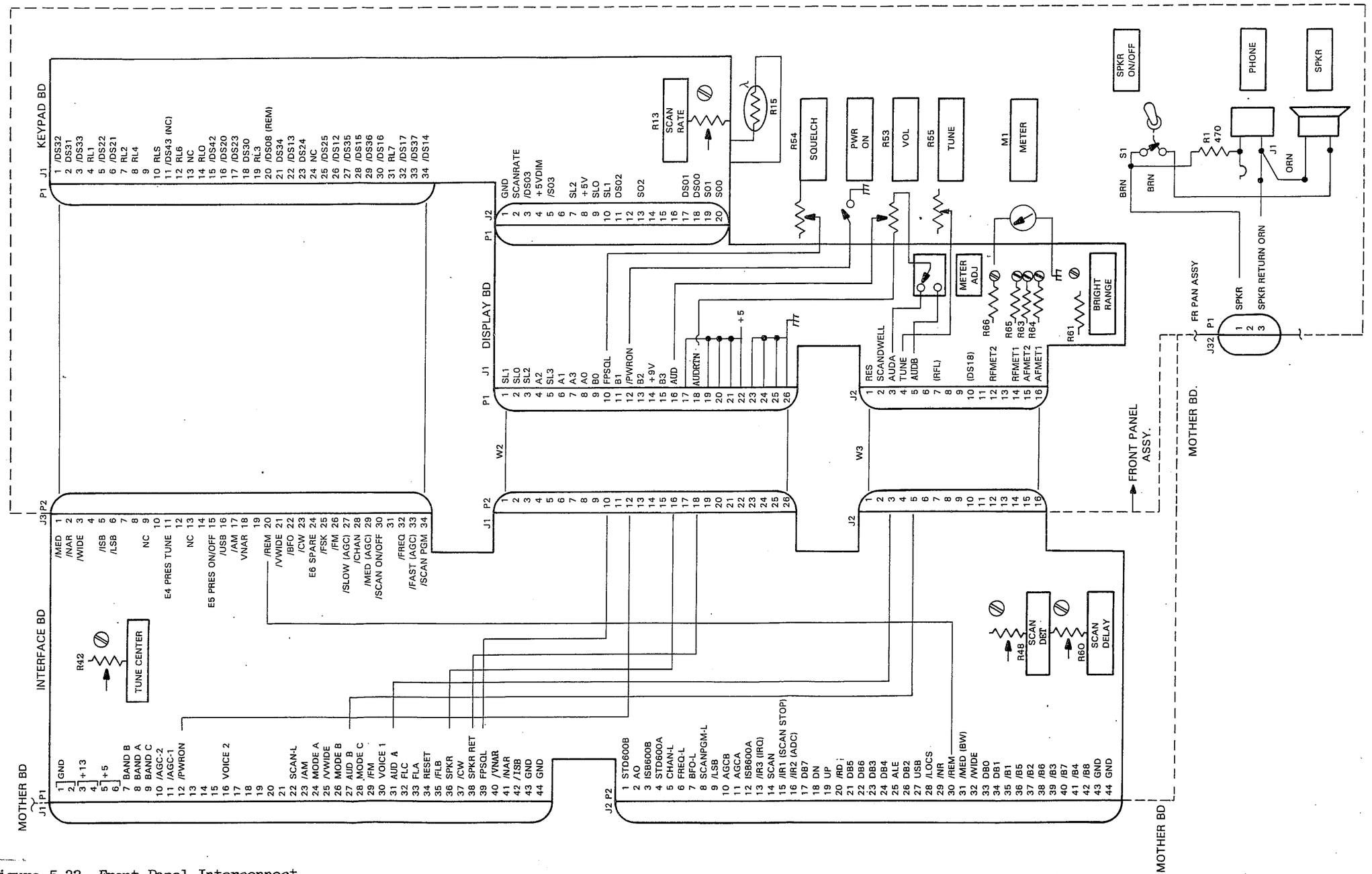


Figure 5.33 Front Panel Interconnect

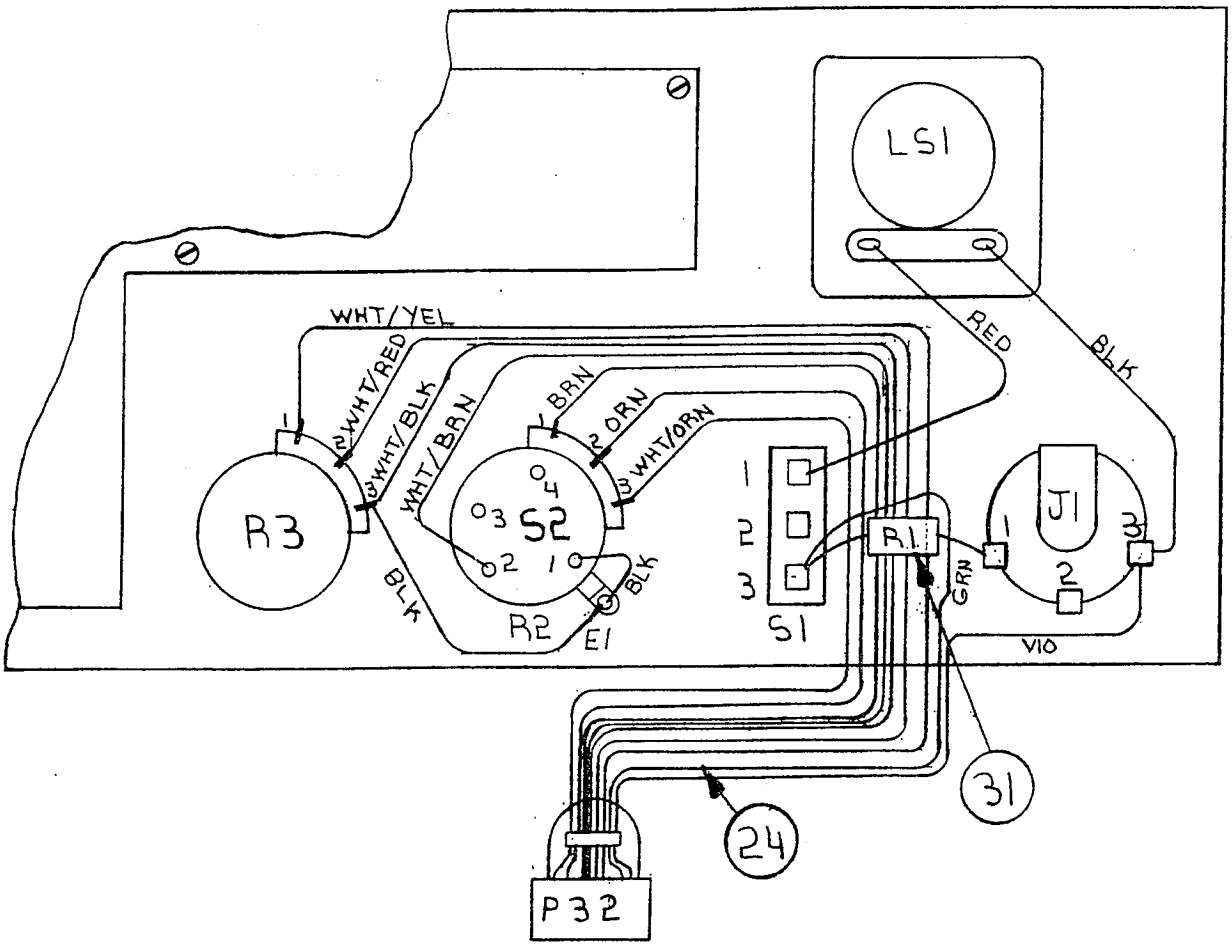


Figure 5.34 Front Panel Wiring Diagram

FRONT PANEL
(600066-539)

SYMBOL	DESCRIPTION	PART NUMBER
J1	Jack, phone	600079-611-002
LS1	Speaker	600008-370-001
P32	Cable, speaker	600522-540-001
R1	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R2/S2	Volume pot	600109-360-002
	Spring, tuning pot return	600014-246-001
	Plate, speaker	603865-602-001
R3	Squelch pot	600110-360-001
S1	Switch, speaker	600213-616-001
	Handle	600262-618-001
	Knob, 7/8 dia.	600101-618-001
	Knob, tuning	600101-618-003
	Brkt., knob return	603242-602-001
	Cloth, grill	600023-641-001

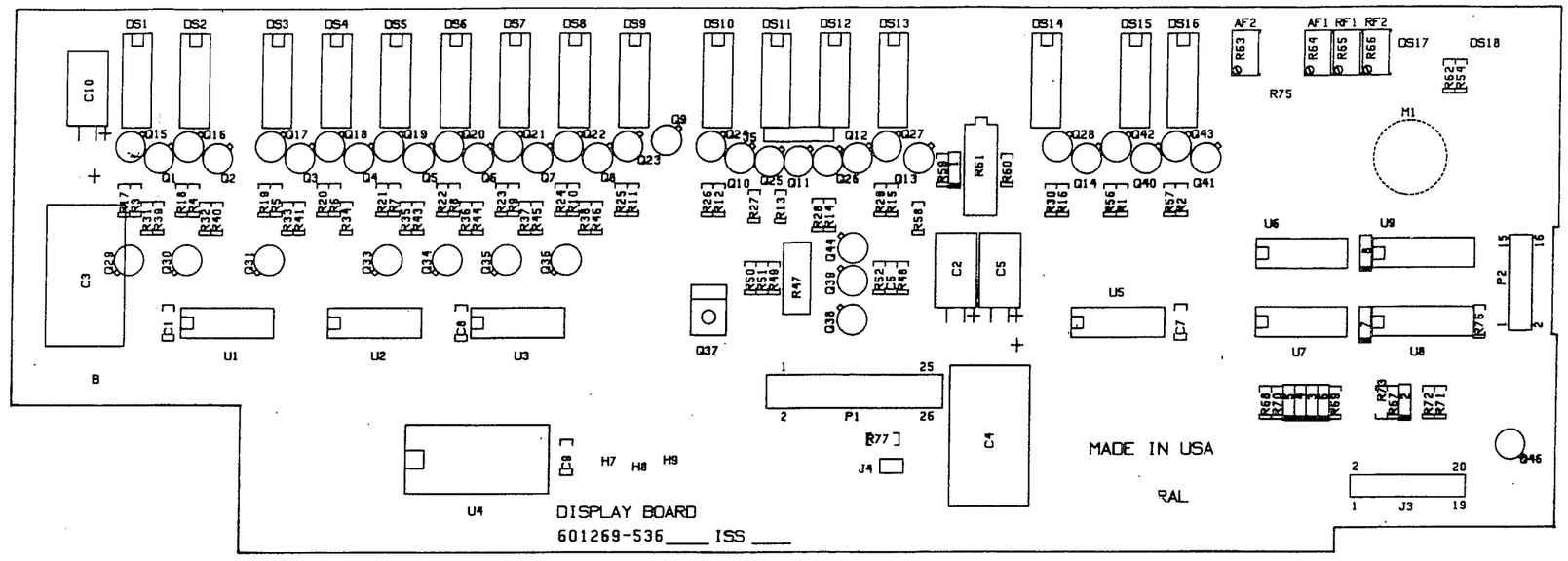
5.17.1 DISPLAY BOARD, 1A21A1

This board receives signals from the interface board to display channel, frequency, emission mode, bite, radio set and meter read out.

Display coded signals from the interface board are applied to U4, pins 20-23. U4 decodes these signals and drives one of the 16-digit drivers to turn on one display at one time. U1, U2, U3 and U5 are inverter drivers to provide enough current to drive digit drivers pairs Q1-28 and 40-43. The 7-segment display signals from the interface board are applied to U1, U2 and U3 inverter drivers which drive Q29-31 and Q33-36.

Flip-flop U8 and U9 control the operation of bilateral switches U6 and U7 which direct inputs to the meter and speaker amplifier. Momentary grounds on inputs to U8 from switches on the keypad board (USB and LSB) toggle the flip-flops to turn on switches in U7 to connect either USB or LSB-derived audio or RF meter signals to U6 which in turn connects either the audio or RF meter signals to the meter as controlled by U9 flip-flop; U9 also being toggled by switches on the keypad board (AF and RF). Two switches in U6, also controlled by the USB/LSB function of U8 select; either USB-derived audio (AUDIO A) or LSB-derived audio (AUDIO B) to be ultimately routed to the speaker amplifier. Both USB and LSB signals are only available with the ISB radio option. Normally only the USB signals are present. When ISB is not selected in the radio, a TTL high exists on J1-18 (ISB) which conditions the S and R of both sections of U8 via Q46 to only allow USB-derived signals to be selected (AUDIO A, RF1 and AF1). The $\overline{Q}$ outputs of U8 and U9 are used to light the LEDs in the initiating switches on the keypad board as the Q outputs control the corresponding switch function in U6 and U7.

The dimmer circuit consists of a photoconductive cell R75 and associated regulating circuitry including Q44 and Q37-39. R75, exposed to ambient lighting through a window in the front panel, varies the bias voltage to Q44. R61 limits the range of brightness control caused by R75.



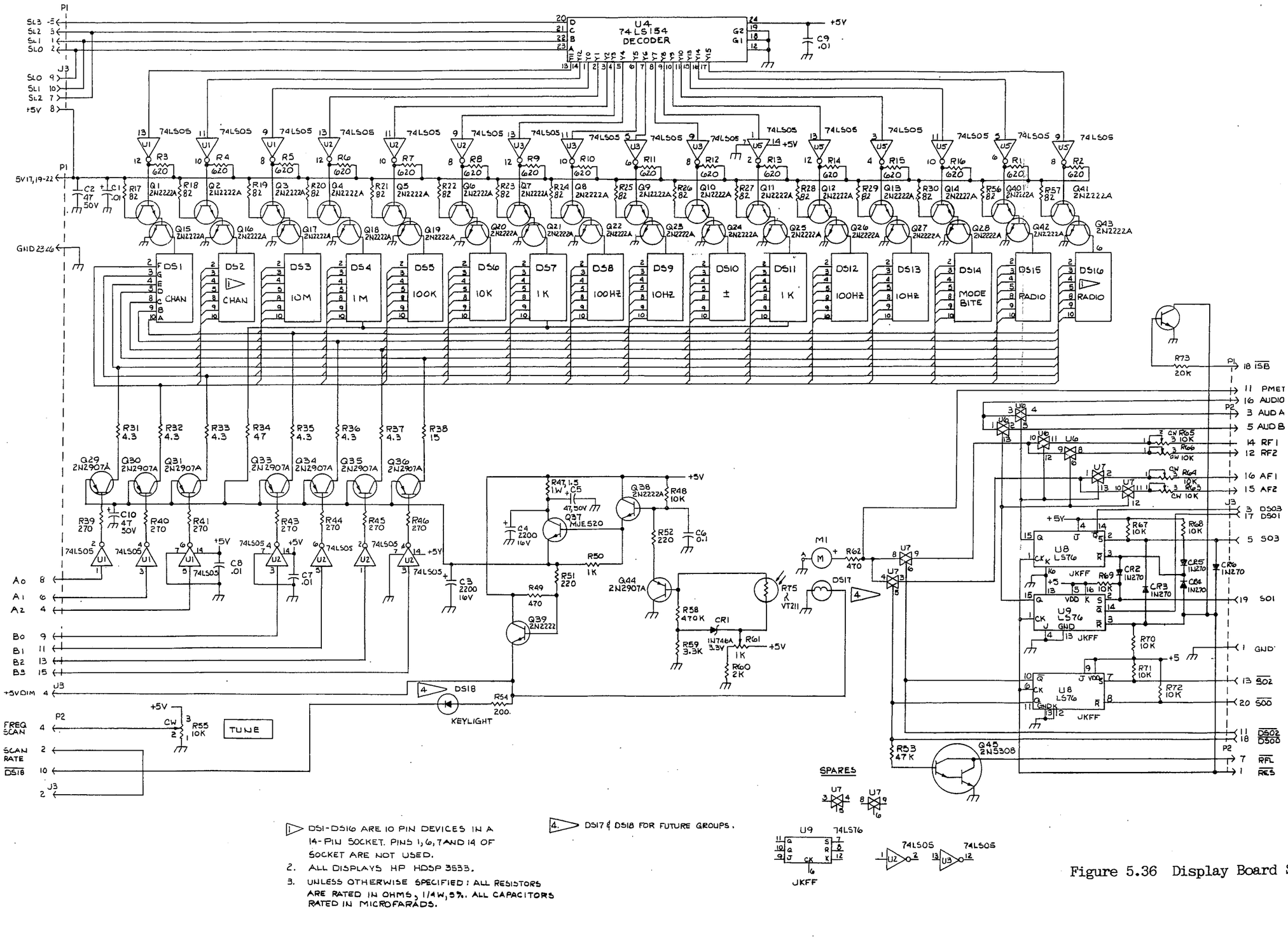
DISPLAY BOARD
(601269-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1,7,8,9	Capacitor, .01µf, 50V	600272-314-002
C2,5,10	Capacitor, 47µf, 50V	600297-314-026
C3.4	Capacitor, 2200µf, 16V	600297-314-040
C6	Capacitor, .1µf, 50V	600272-314-001
CR1	Zener, 1N746, 3.3V	600002-411-001
CR2-6	Diode, 1N270	600052-410-001
DS1-16	LED, HDSP3533	600550-415-002
(DS1-16)	Elev. socket	600126-419-006
J3	Connector, 20 pin	600174-608-014
M1	Meter, 0-1mA	600034-368-003
P1	Cable assembly, 26 pin	600476-540-010
P2	Cable assembly, 16 pin	600476-540-009
Q1-28,38-43, 46	Transistor, 2N2222A	600080-413-001
(Q1-31,33-36, 38-44,46)	Transistor pad	600025-419-001
Q29-31,33-36, 44	Transistor, 2N2907A	600154-413-001
Q37	Transistor, MJE520 7806/1	600220-413-001
Q45	Transistor, 2N5308 413-001	600221-413-002

DISPLAY BOARD
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
R1-16	Resistor, 620Ω, 1/4W, 5%	662004-341-075
R17-30,56,57	Resistor, 82Ω, 1/4W, 5%	682094-341-075
R31-33,35-38	Resistor, 4.3K, 1/4W, 5%	643084-341-075
R34	Resistor, 47Ω, 1/4W, 5%	647094-341-075
R39-41,43-46	Resistor, 270Ω, 1/4W, 5%	647004-341-075
R47	Resistor, 1.5K, 1W, 5%	615084-341-325
R48,67-72	Resistor, 10K, 1/4W, 5%	610024-341-075
R49,62	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R50	Resistor, 1K, 1/4W, 5%	610014-341-075
R51,52	Resistor, 220Ω, 1/4W, 5%	622004-341-075
R53	Resistor, 47K, 1/4W, 5%	647024-341-075
R54	Resistor, 200Ω, 1/4W, 5%	620004-341-075
R55	Pot, 10K	600115-360-002
R58	Resistor, 470K, 1/4W, 5%	647034-341-075
R59	Resistor, 3.3K, 1/4W, 5%	633014-341-075
R60	Resistor, 2K, 1/4W, 5%	620014-341-075
R61	Pot, 1K	600063-360-007
R63-66	Pot, 10K	600098-360-010
R73	Resistor, 20K, 1/4W, 5%	620024-341-075
R75	LDR, VT211	600013-373-001
U1-3,5	IC, 74LS05	600240-415-001
U4	IC, 74LS154	600412-415-001
U6,7	IC, 4066	
U8,9	IC, 74LS76	600545-415-001

Figure 5.35 Display Board Assembly



1. DS1-DS16 ARE 10 PIN DEVICES IN A 14-PIN SOCKET. PINS 1, 6, 7 AND 14 OF SOCKET ARE NOT USED.
2. ALL DISPLAYS HP HDSP 3533.
3. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE RATED IN OHMS, 1/4W, 5%. ALL CAPACITORS RATED IN MICROFARADS.
4. DS17 & DS18 FOR FUTURE GROUPS.

Figure 5.36 Display Board Schematic

DISPLAY BOARD

1A1A21A1

Pin Connections and Voltage Readings

1A1A21A1P1

SL1	◎ 1	2 ○		SL0
SL2	○ 3	4 ○		A2
SL3	○ 5	6 ○		A1
	○ 7	8 ○		A0
B0	○ 9	10 ○		
B1	○ 11	12 ○		
B2	○ 13	14 ○		
B3	○ 15	16 ○		AUDIO 0-150 MV
+5V	○ 17	18 ○		$\overline{\text{ISB}}$
+5V	○ 19	20 ○		+5V
+5V	○ 21	22 ○		+5V
GND	○ 23	24 ○		GND
GND	○ 25	26 ○		GND
	○ 27	28 ○		
	○ 29	30 ○		
	○ 31	32 ○		
	○ 33	34 ○		
	○ 35	36 ○		
	○ 37	38 ○		
	○ 39	40 ○		
	○ 41	42 ○		
	○ 43	44 ○		

BOTTOM VIEW

DISPLAY BOARD

1A1A21A1

Pin Connections and Voltage Readings

1A1A21A1P2

		1	2	SCAN RATE
0-150mVAC AUD A		3	4	FREQ SCAN 0-5 VDC
0-150mVAC AUD B		5	6	
		7	8	
		9	10	DS 18
		11	12	RF1 2-6 VDC
		13	14	RF1 2-6 VDC
0- 2 VDC AF2		15	16	AF1 0-2 VDC
		17	18	
		19	20	
		21	22	
		23	24	
		25	26	
		27	28	
		29	30	
		31	32	
		33	34	
		35	36	
		37	38	
		39	40	
		41	42	
		43	44	

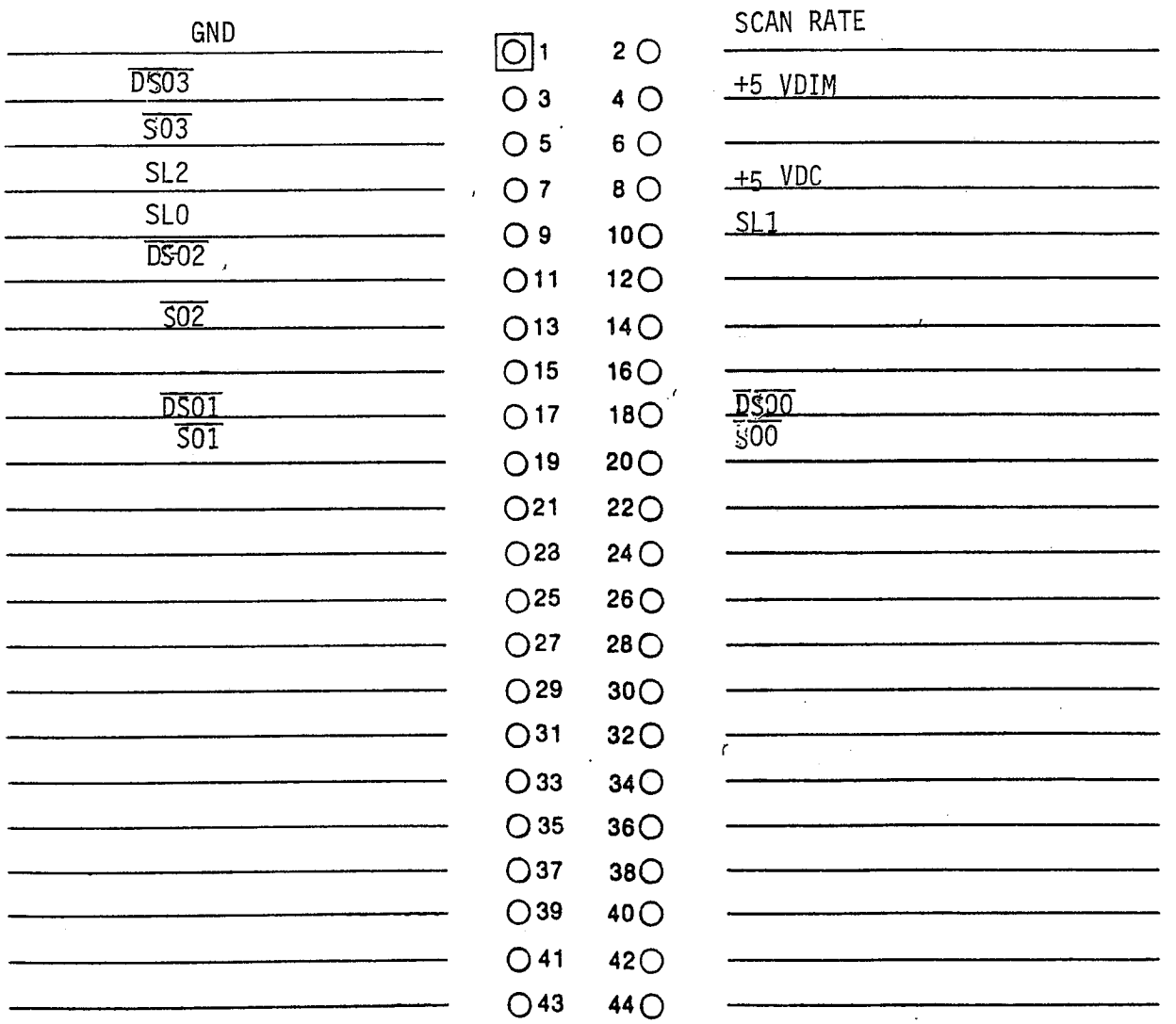
BOTTOM VIEW

DISPLAY BOARD

1A1A21A1

Pin Connections and Voltage Readings

1A1A21A1J3



5.17.2 KEYPAD BOARD, 1A1A21A2

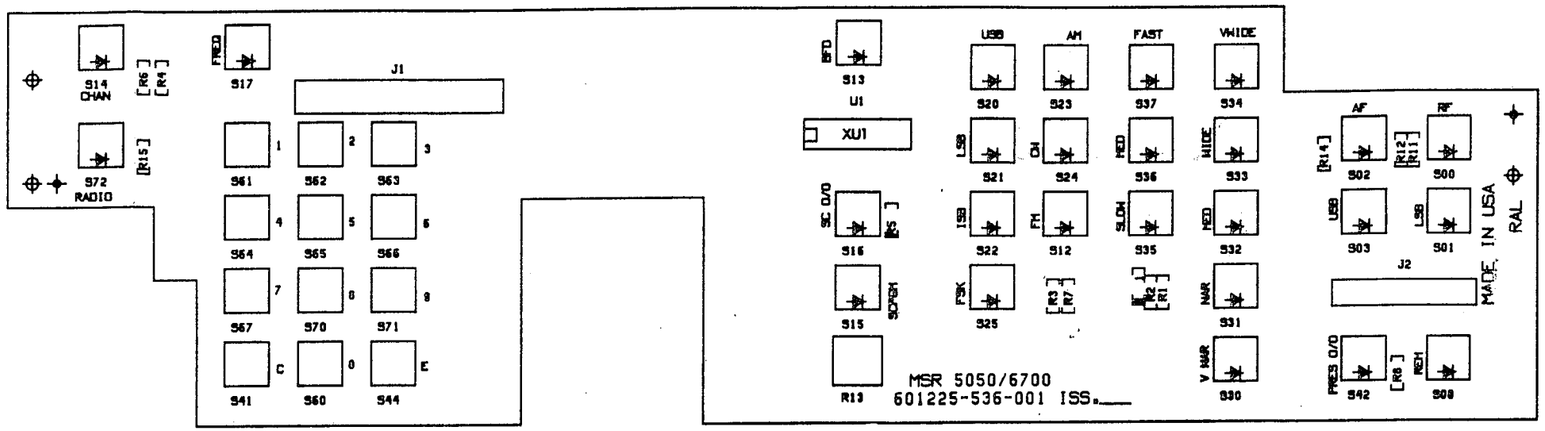
The keypad board contains 34 momentary pushbutton switches (S12-17, 20-25, 30-37, 41, 42, 44, 60-67 and 70-72) which are connected in a matrix which send pulses to the interface board when a key is pressed.

Switches S60-67, 70 and 71 are designed for numbers 0 to 9. Switch S41 is for the letter "C" and S44 is for the letter "E". Switches S12-17, 20-25, 30-37, 42 and 72 have LEDs mounted in the keycaps that light when the key is pressed to indicate that its particular function (chan., freq., BFO, scan on/off, scan prog., mode, AGC, filter, presel on/off or radio set) is engaged.

Switches S00-03 and 08 are not connected in the matrix. Switch S02 selects AF and S00 selects RF on the front panel meter. Switch S03 selects USB and S01 selects LSB when the radio is in the ISB mode. Switch S08 is an alternate action switch which conditions the radio for remote control operation.

U1 decodes the three least significant scan lines (SL0, SL1 and SL2) from the 8279 keyboard IC on the interface board to produce 6 scan lines in the keypad board switch matrix.

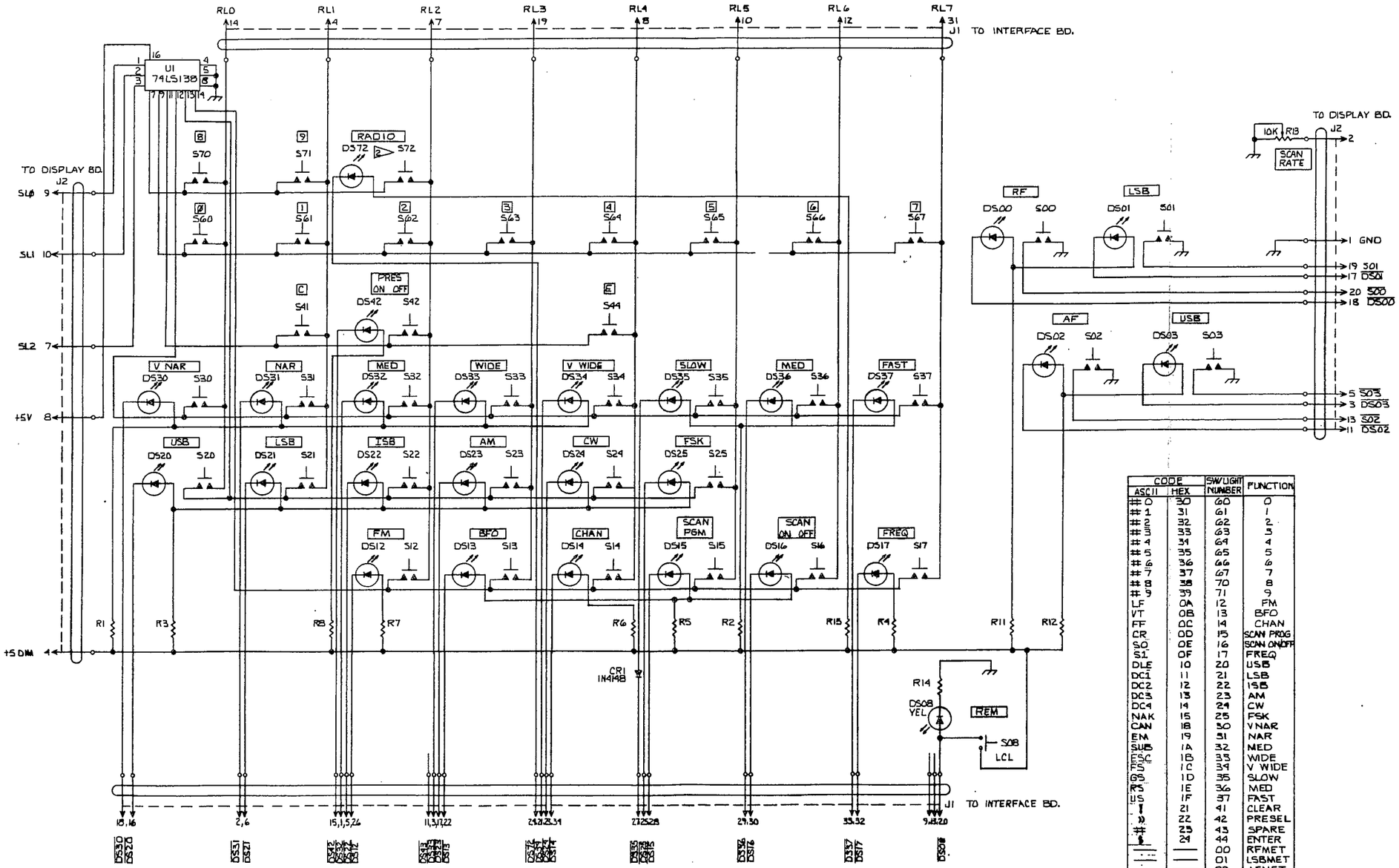
R13, mounted on the keypad board to allow easy front panel adjustment, controls the speed of the scan rate oscillator on the interface board.



KEYPAD BOARD
(601225-536)

SYMBOL	DESCRIPTION	PART NUMBER
CR1	Diode, 1N4148	600109-410-001
J1	Cable assembly, 34 pin	600476-540-012
J2	Cable assembly, 20 pin	600476-540-011
R1-8,11, 12,14,15	Resistor, 130Ω, 1/4W, 5%	613004-341-075
R13	Resistor, Var., 10K	600072-360-010
S00-03,13-17,42	Mom. switch assy., lit	600314-616-602
S08	Alt. switch assy.,lit	600314-616-603
S12,20-25, 30-37	Mom. switch assy.,lit	600314-616-601
S41 "C"	Switch assy., engraved	600318-616-012
S44 "E"	Switch assy., engraved	600318-616-011
S60 "0"	Switch assy., engraved	600318-616-010
S61 "1"	Switch assy., engraved	600318-616-001
S62 "2"	Switch assy., engraved	600318-616-002
S63 "3"	Switch assy., engraved	600318-616-003
S64 "4"	Switch assy., engraved	600318-616-004
S65 "5"	Switch assy., engraved	600318-616-005
S66 "6"	Switch assy., engraved	600318-616-006
S67 "7"	Switch assy., engraved	600318-616-007
S70 "8"	Switch assy., engraved	600318-616-008
S71 "9"	Switch assy., engraved	600318-616-009
U1	IC, 74LS138	600309-415-001
XU1	IC, socket	600206-419-016

Figure 5.37 Keypad Board Assembly



CODE ASCII	CODE HEX	SW/LIGHT NUMBER	FUNCTION
#0	30	60	0
#1	31	61	1
#2	32	62	2
#3	33	63	3
#4	34	64	4
#5	35	65	5
#6	36	66	6
#7	37	67	7
#8	38	70	8
#9	39	71	9
LF	0A	12	FM
VT	0B	13	BFO
FF	0C	14	CHAN
CR	0D	15	SCAN PROG
SO	0E	16	SCAN ON/OFF
SI	0F	17	FREQ
DLE	10	20	USB
DC1	11	21	LSB
DC2	12	22	ISB
DC3	13	23	AM
DC4	14	24	CW
NAK	15	25	FSK
CAN	18	30	V NAR
EM	19	31	NAR
SUB	1A	32	MED
ESC	1B	33	WIDE
FS	1C	34	V WIDE
GS	1D	35	SLOW
RS	1E	36	MED
US	1F	37	FAST
!	21	41	CLEAR
"	22	42	PRESEL
#	23	43	SPARE
$	24	44	ENTER
		00	RFMET
		01	LSBMET
		02	AFMET
		03	USBMET
	3A	72	SPARE
		08	REMOTE

NOTES

1. ALL RESISTORS ARE 130 OHMS, 1/4W, 5%.

2 DS72 AND S72 ARE FOR FUTURE GROUPS.

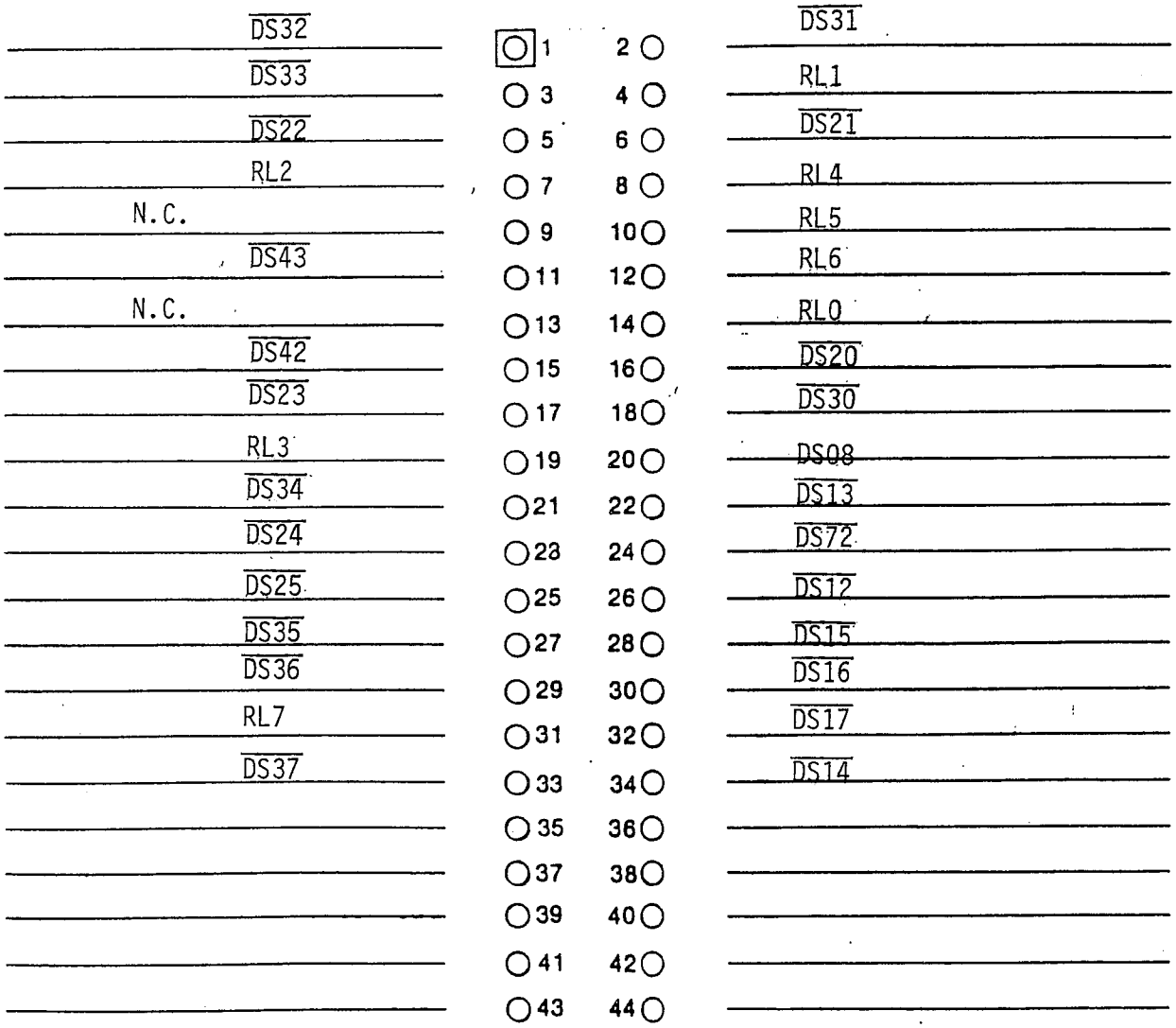
Figure 5.38 Keypad Board Schematic

KEYPAD BOARD

1A1A21A2

Pin Connections and Voltage Readings

1A1A21A2P1



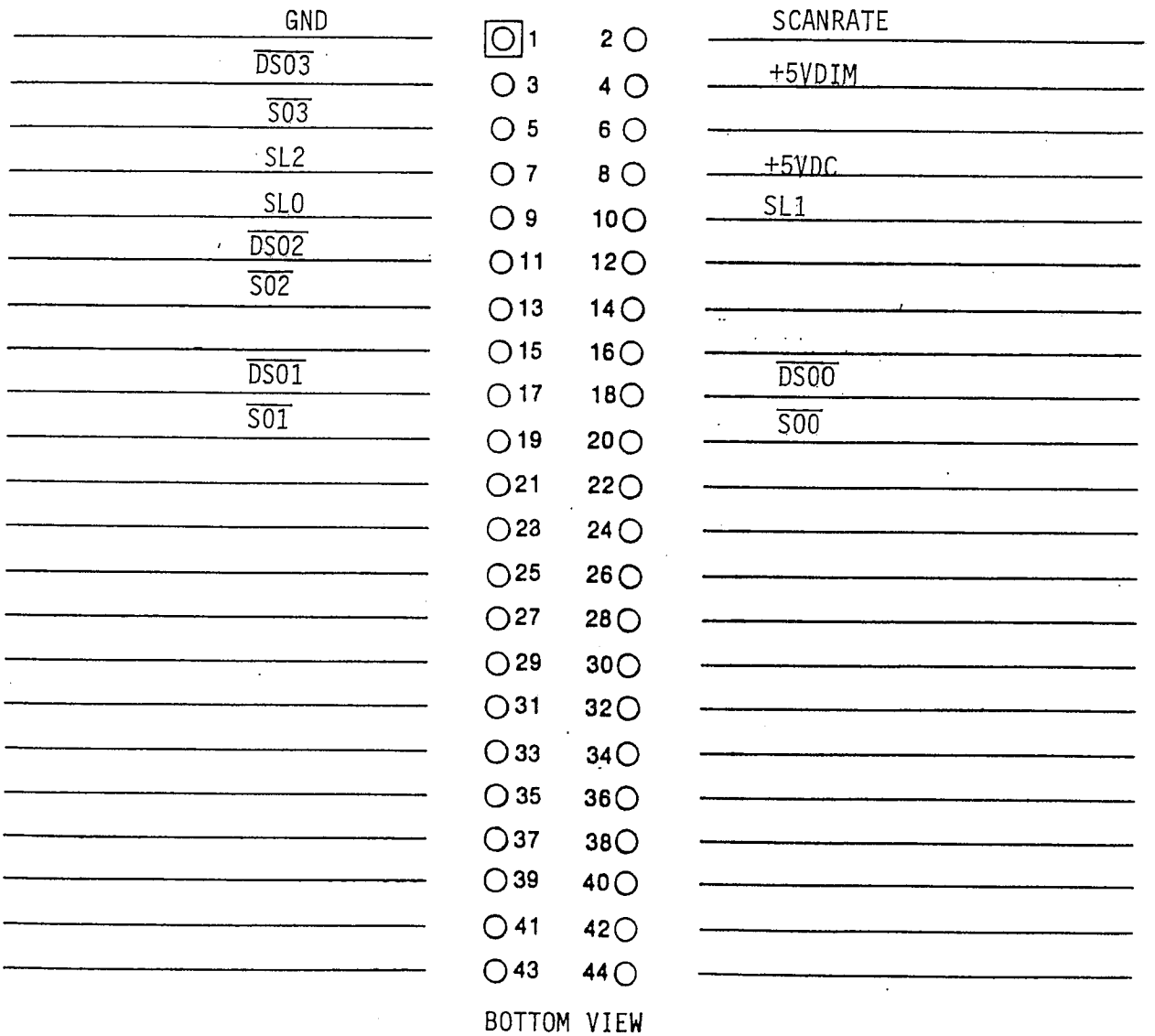
BOTTOM VIEW

KEYPAD BOARD

1A1A21A2

Pin Connections and Voltage Readings

1A1A21A2J2

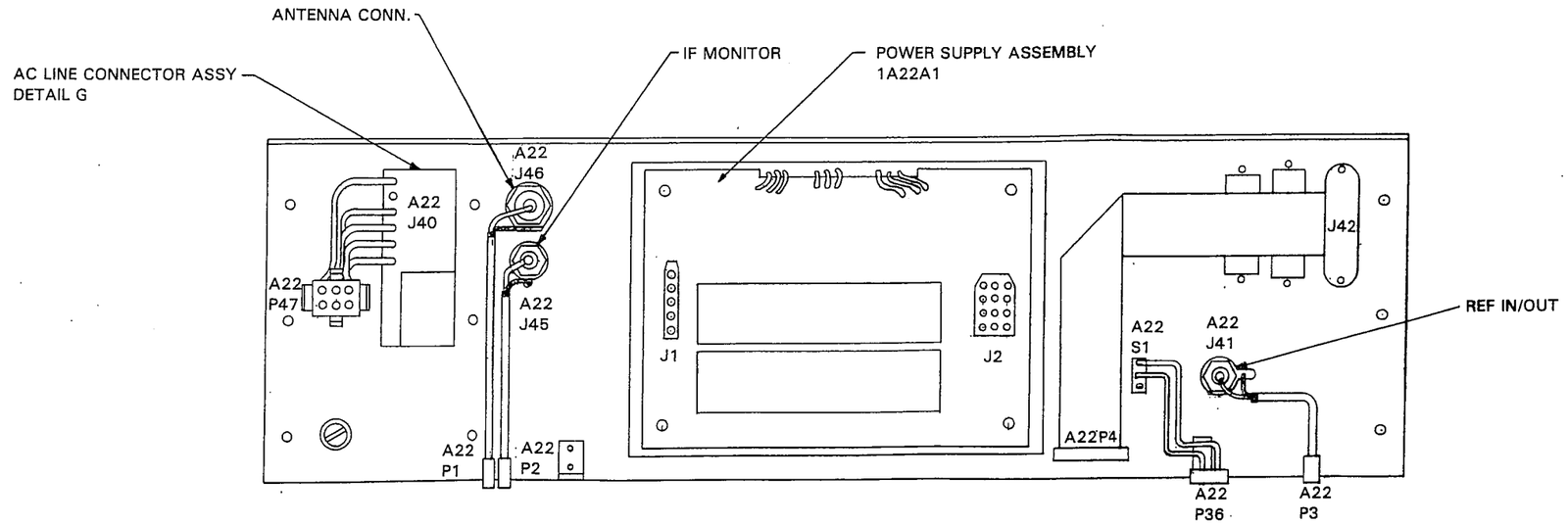


BOTTOM VIEW

5.18 REAR PANEL ASSEMBLY, 1A22

The rear panel, Figures 53.9, 5.40 and 5.41 contains the power supply and connectors for external interface. It is detachable from the main receiver by 11 screws. Electrical disconnect is by 6 connectors from the mother board, 1A4 and by 2 molex connectors to the left side support assembly which contains the power transformer and low-voltage rectifiers for the preregular circuits.

The AC power is brought in through J40 which contains the fuse, line filter and a voltage selector card, which interconnects transformer windings to adapt to various line voltages. J46, J45 and J41 are coax connectors for antenna, 5 MHz IF monitor and 5MHz reference signals. S1 provides a selectable ground to the reference board 1A9, to allow synthesizer operation from an external reference or internal reference using J41. J42 contains line audio outputs and miscellaneous inputs and outputs (see Figure 5.41). The power supply 1A22A1 is detachable by 4 screws. It supplies the DC requirements of the radio.



REAR PANEL
(600069-539)

SYMBOL	DESCRIPTION	PART NUMBER
	Ground lug	600206-230-020
J40	AC filter/connector	600070-529-001
J41,45	Connector, BNC	600052-606-001
J42	Cable assy., sub. min.	600476-540-008
	Cable assy., ref. sw.	600567-540-001
J42	Mounting kit	600116-204-001
J46	Connector, UG239	600373-606-001
J47	Cable assy., line pwr.	600559-540-001
S1	Switch, int./ext.	600213-616-001

Figure 5.39 Rear Panel Assembly Interior

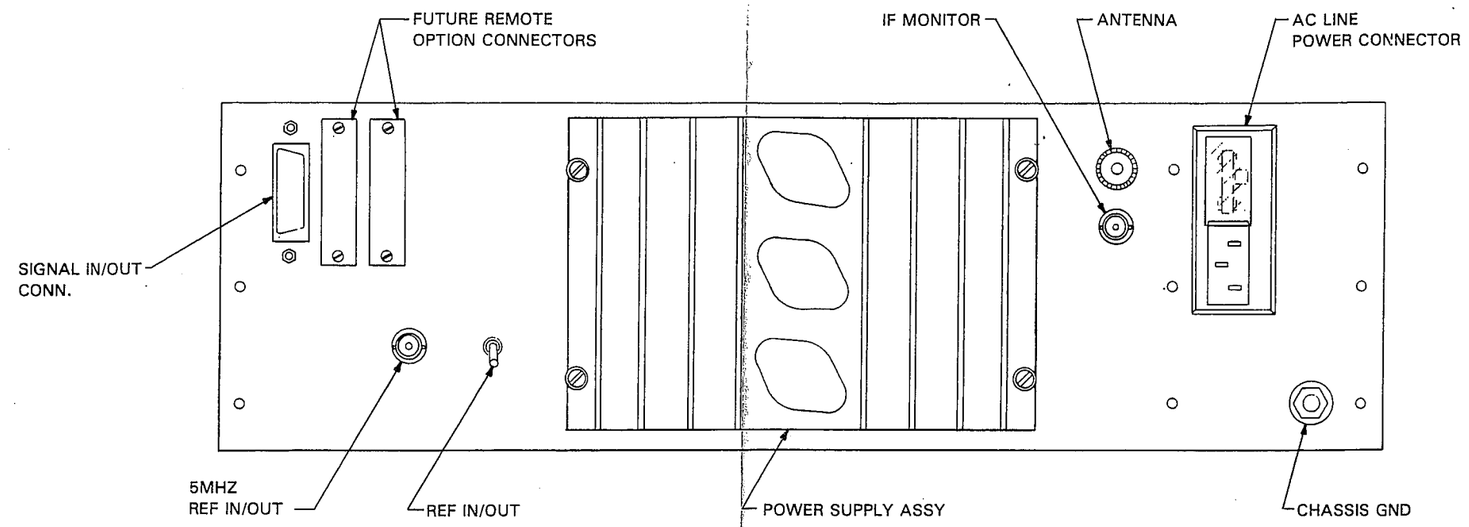


Figure 5.40 Rear Panel Assembly Exterior

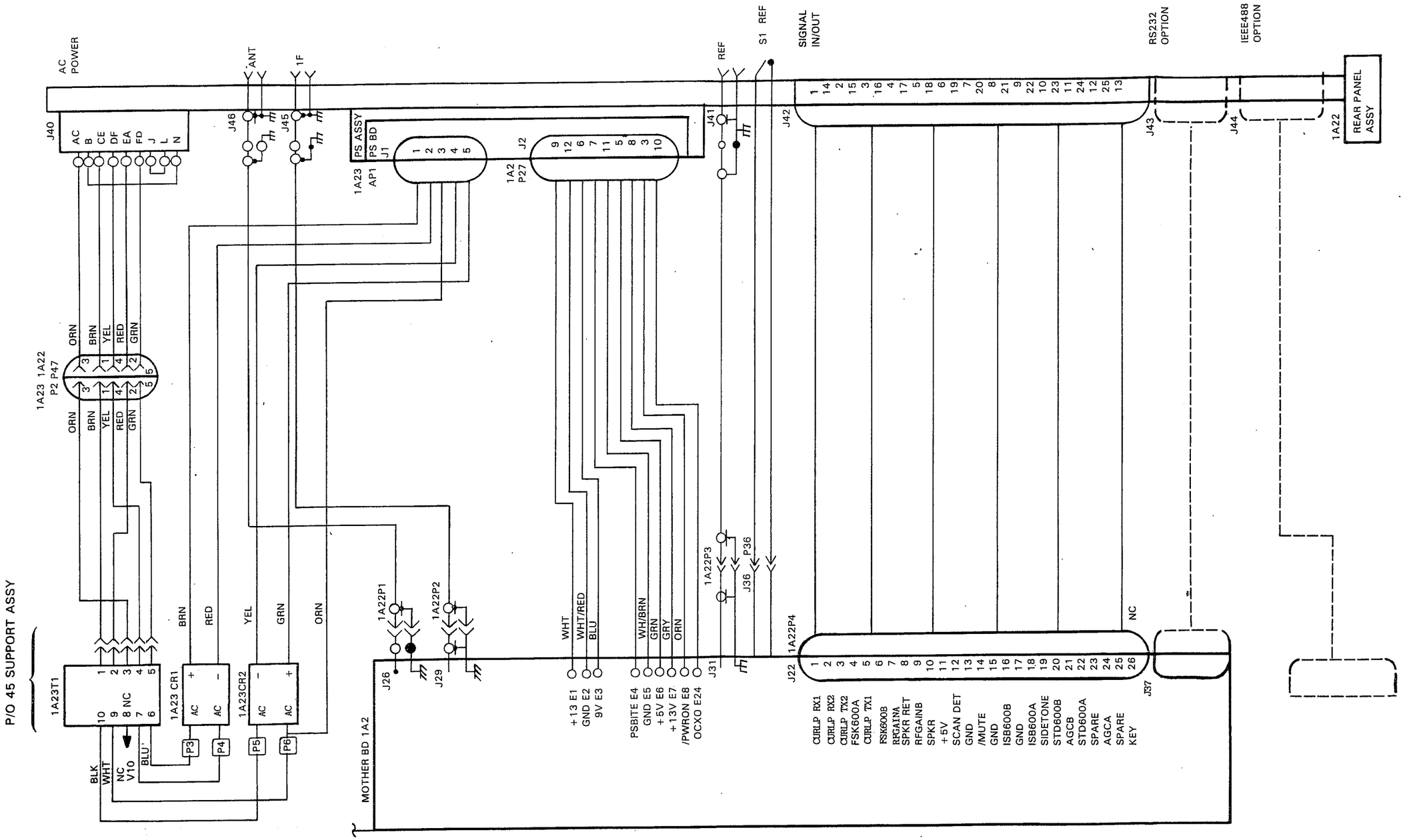


Figure 5.41 Rear Panel Interconnect

5.18.1 POWER SUPPLY ASSEMBLY, 1A21A1

The power supply consists of a printed circuit board (containing regulators and associated circuitry) mounted to a heatsink to which the pass transistors for the series regulator circuits are attached. U1 supplies the 13 VDC output by controlling the pass transistor Q1 via U1-11 to maintain 7.15 VDC at U1-4. The ratio of resistors R6 and R7 determine the ratio of the output voltage to U1-4. The 9-volt supply is provided by U2 and Q2 in the same manner, with a different ratio of resistors (R13 and R14) determining the ratio of 7.15 VDC to 9 VDC.

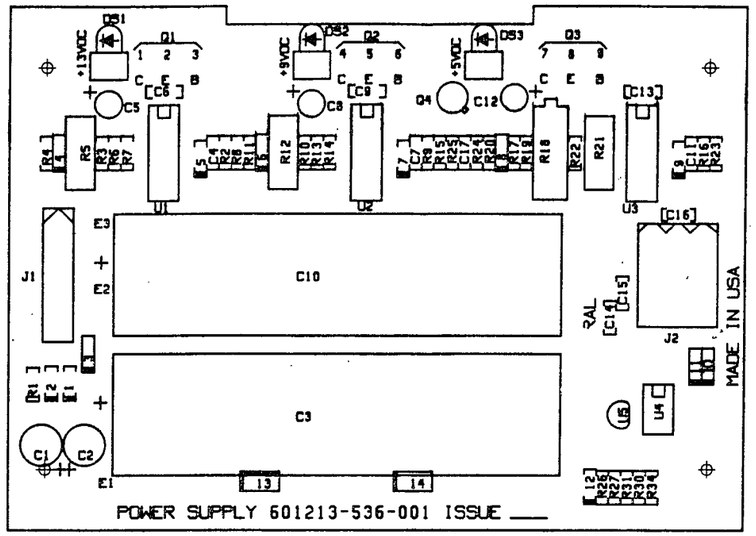
R5 and R12 are the current limiting resistors for U1 and U2 which limit the 13 volts to 2 amps and the 9 volts to 1.4 amps. The input supply for the 13 and 9-volt regulators is a full wave rectified output from a 16.5 VRMS transformer. C3 smooths the ripple to about 1 volt RMS. To increase the low line operating range, the 16.5 VRMS AC signal (J1-3) is doubled and clamped to the normal preregulated input (J1-5) so that U1 always has a high supply voltage. CR3 limits the maximum voltage to U1-12.

U3 supplies an adjustable 5-volt output by varying the reference input to U3-5 via R18. The output current is limited to 2.7 amps by R21. The power input (J1-1) is obtained by full wave rectifying a 10 VRMS AC transformer output. C10 reduces the ripple to 1 VRMS. The supply voltage for U3 (pin D) is obtained from the 13-volt preregulated input (20 VAC nominal) to allow low line operation.

An on-board BITE indication is produced by DS1, DS2, DS3 and associated current-limiting resistors and zeners to indicate the presence of the 13, 9 and 5-volt outputs. An additional off-board BITE signal is produced by U4 and associtaed circuitry which detects a drop of 10 percent in the 9 or 13-volt supply to produce a logic 0 output on J2-1.

The power supply outputs are enabled by a logic 0 on J2-3 which removes the grounds on U1, 2 and 3 (pin 13) via Q4.

A frequency reference oven supply voltage is provided at J2-10 which maintains a nominal 12.6 VDC output anytime preregulated power is provided to the board. When the outputs are disabled, the preregulated voltage at J1-5 increases to 24 volts because of the reduced loading. CR13 and CR14 drop the voltage by 11.2V to 12.8 VDC. When the outputs are enabled, the voltage reduces to 8.8 VDC from CR13 and CR14 but the 13-volt output overrides this through CR12 providing 12.4 VDC to J2-10.



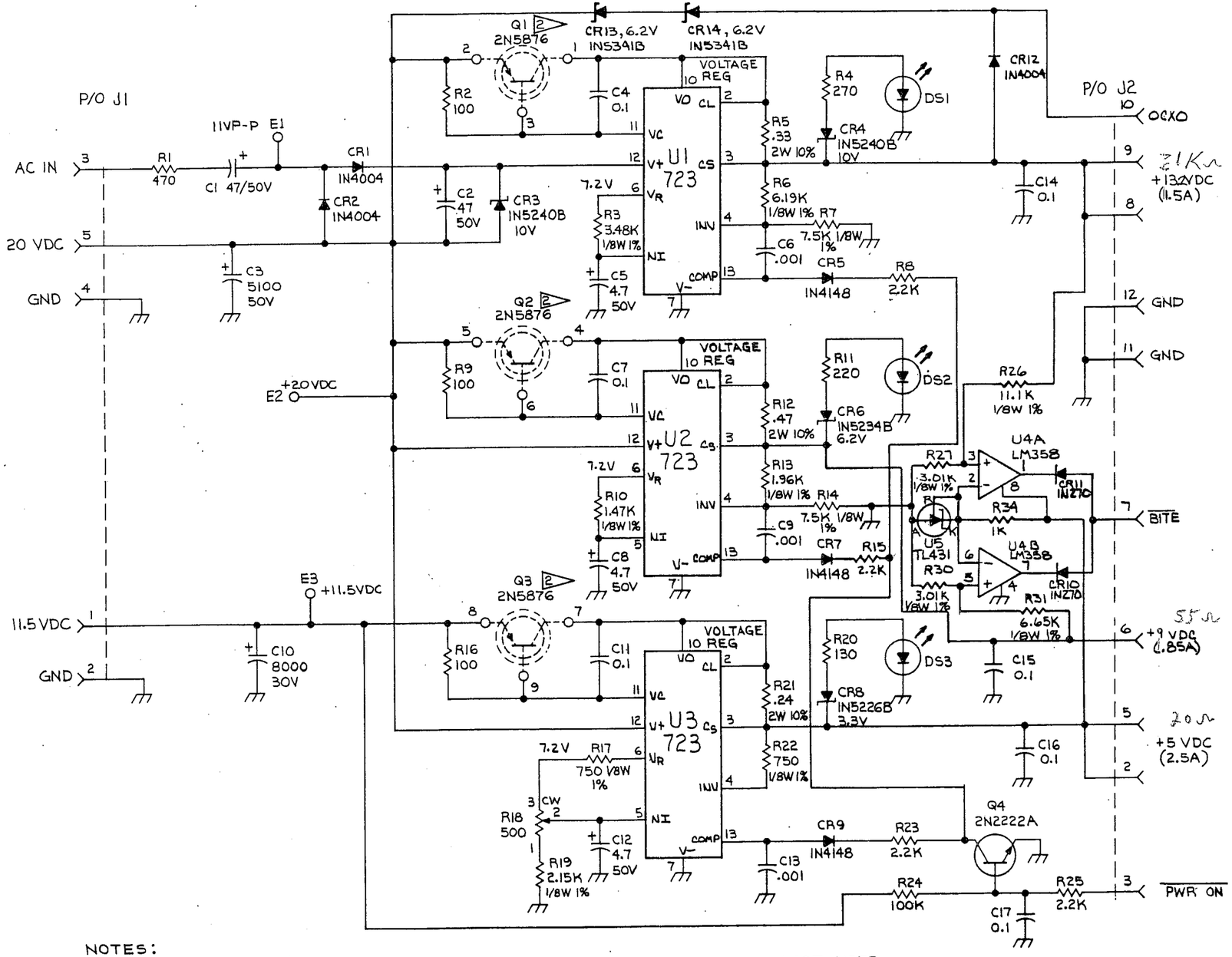
POWER SUPPLY
(601213-536)

SYMBOL	DESCRIPTION	PART NUMBER
C1,2	Capacitor, 47µf, 50V	600297-314-026
C3	Capacitor, 5100µf, 50V	600309-314-001
C4,7,11 14-17	Capacitor, .1µf, 50V	600272-314-001
C5,8,12	Capacitor, 4.7µf, 50V	600297-314-010
C6,9,13	Capacitor, .001µf, 50V	600272-314-004
C10	Capacitor, 8000µf, 30V	600309-314-002
CR1,2,12	Diode, 1N4004	600011-416-002
CR3,4	Zener, 1N5240B, 10V	600033-411-020
CR5,7,9	Diode, 1N4148	600109-410-001
CR6	Zener, 1N5234B, 6.2V	600033-411-014
CR8	Zener, 1N5226B, 3.3V	600033-411-006
CR10,11	Diode, 1N270	600052-410-001
CR13,14	Zener, 1N5341B	600026-411-009
DS1,2,3	LED, yellow	600043-390-002
E1,2,3	Terminal	600261-230-001
	Transistor pad	600025-419-001
	Mount, LED	600005-635-001
J1	Connector, 5 pin	600237-608-003
J2	Connector, 12 pin	600237-608-001
Q4	Transistor, 2N2222A	600080-413-001

POWER SUPPLY
(cont.)

SYMBOL	DESCRIPTION	PART NUMBER
R1	Resistor, 470Ω, 1/4W, 5%	647004-341-075
R2,9,16	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R3	Resistor, 3.48K, 1/8W, 1%	634811-342-059
R4	Resistor, 270Ω, 1/4W, 5%	627004-341-075
R5	Resistor, .33Ω, 2W, 10%	600057-340-002
R6	Resistor, 6.19K, 1/8W, 1%	661911-342-059
R7,14	Resistor, 7.50K, 1/8W, 1%	675011-342-059
R8,15,23, 25	Resistor, 2.2K, 1/4W, 5%	622014-341-075
R10	Resistor, 1.47K, 1/8W, 1%	614711-342-059
R11	Resistor, 220Ω, 1/4W, 5%	622004-341-075
R12	Resistor, .47Ω, 2W, 10%	600057-340-004
R13	Resistor, 1.96K, 1/8W, 1%	619611-342-059
R17,22	Resistor, 750Ω, 1/8W, 1%	675001-342-059
R18	Pot, 500Ω	600063-360-006
R19	Resistor, 2.15K, 1/8W, 1%	621511-342-059
R20	Resistor, 130Ω, 1/4W, 5%	613004-341-075
R21	Resistor, .24Ω, 2W, 5%	600057-340-017
R24	Resistor, 100K, 1/4W, 5%	610034-341-075
R26	Resistor, 11.1K, 1/8W, 1%	611121-342-059
R27	Resistor, 3.01K, 1/8W, 1%	630111-342-059
R31	Resistor, 6.65K, 1/8W, 1%	666511-342-059
R34	Resistor, 1K, 1/4W, 5%	610014-341-075
U1,2,3	IC, MC1723L	600040-415-101
U4	IC, LM358	600150-415-001
U5	IC, TL431ILP	600632-415-001

Figure 5.42 Power Supply Assembly



NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS RATED IN MICROFARADS AND ALL RESISTORS ARE RATED IN OHMS, 1/4 WATT, 5%.
2. FUTURE CONNECTIONS SHOWN FOR REFERENCE ONLY. COMPONTS NOT PART OF THIS UNIT.

LAST USED

C17
E3
Q4
R34
U5
CR14

Figure 5.43 Power Supply Schematic

ADDENDUM

TITLE : MSR 5050 OPERATION AND MAINTENANCE MANUAL

PUBLICATION NO: 600249-823-001

PUBLICATION ISSUE NO: 1

ADDENDUM NO: 3

DATE OF ISSUE: August, 1988

This addendum is included as part of the MSR 5050 manual to provide information on MSR 5050 receivers supplied with the later configuration PC board assemblies listed below.

ASSEMBLY	PART NUMBER
Interface Board	601180-536-003
IF Filter Board	601076-536-010
Audio Squelch Board	601077-536-004, or -005

1.1 GENERAL

The PC assemblies listed above form a complementary board set and should not be interchanged with PC assemblies having different part numbers.

1.1.1 MANUAL CHANGES

The following pages in the manual and Addendum #2 of the manual change due to the new boards and are supplied with this addendum: 5-13 and 5-14 of the manual and 2-1, 2-2, 4-1, and 4-2 of Addendum #2.

2.1 SQUELCH SPECIFICATIONS

The PC assemblies listed above provide the MSR 5050 with syllabic squelch capability with adjustable carrier squelch.

2.1.1 SYLLABIC SQUELCH

Operates on signals typically greater than 2 µV having syllabic voice characteristics; generally independent of signal strength. Refer to Table 2.1 for front panel operation.

2.1.2 Carrier Squelch

Carrier squelch operates on signals of approximately 20 µV or greater. Refer to Table 2.1 for front panel operation.

2.1.3 600 Ohm Audio Muting with Squelch

An internal jumper located on the Audio Squelch board 601077-536-004 or -005 allows selectable muting of the 600 ohm audio with squelch operation.

	FULL CCW	← KNOB POSITION →	FULL CW
SYLLABIC SQUELCH	OFF	ON/INDEPENDENT OF POSITION	
CARRIER SQUELCH	OFF	20 mV ← ADJUSTABLE THRESHOLD →	1V

TABLE 2.1 FRONT PANEL SQUELCH OPERATION

IF FILTER OPTION (610083-700)

2.1 GENERAL

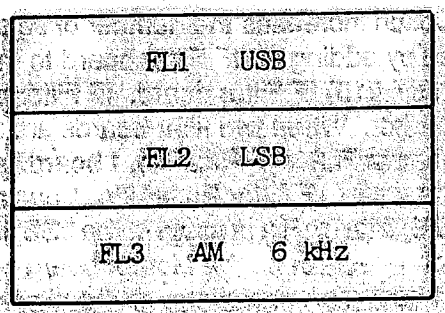
The IF Filter Option increases the number of selectable bandwidths in the MSR 5050 receiver. This is accomplished by adding an IF Filter board to the standard radio which has been previously tested with the standard (-010) IF Filter board. IF Filter board No. 2 has an LSB, a 1 kHz (NAR) filter, and a 400 Hz (VNAR) filter. When two filter boards are used, the LSB filter-enable line addresses FL1 in IF Filter No. 2 instead of FL2 in IF Filter No. 1 board as is the case when the standard (-010) IF Filter board is installed in the radio. IF Filter Board No. 1 has a USB filter in FL1, a 6 kHz (WIDE) filter in FL3, and a 16 kHz (VWIDE) filter in FL2 in place of the LSB filter. This allows the maximum complement of filters. Adding a zero ohm resistor on the Mother board conditions the radio program to enable the additional filter bandwidth controls. Variations to the filter complement are expected in future requirements. Specifications are also detailed with the IF Filter board (601076-536-XXX, Section 5.13) and the MSR 5050 Performance Specifications.

In the IF Filter Option all AM and CW filters are centered on the tuned receiver frequency; when the MED bandwidth key is selected in conjunction with AM, CW or FSK, the USB filter is enabled. The first LO is offset 1.6 kHz low while the frequency display remains unchanged. This centers incoming signals at the indicted frequency in the center of the offset USB filter. For CW and FSK, the BFO is also offset 1.6 kHz low to produce a zero beat for incoming signals at the indicated frequency. For this reason the IF Filter Option must be accompanied by the BFO Option 6000107-700 instead of the fixed 5 MHz, 3rd LO from the Reference board in the standard radio. Figure 1 shows the complements of filters for the Filter Option. Refer to Section 5.13 for detailed information on the IF Filter boards.

2.2 INSTALLATION

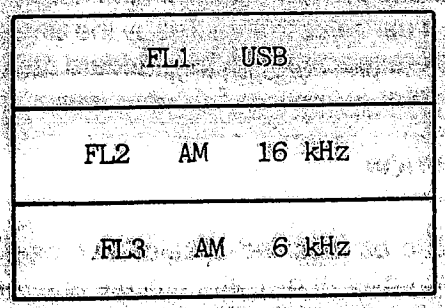
The MSR 5050 to be modified should have been previously tested with a standard IF Filter board. Remove the top cover and shield. Locate and remove jumper JP1 on the Mother board. Add a zero ohm resistor R13 on the Mother board in the position indicated. Plug IF Filter 601076-536-013 into J14. Plug IF Filter 601076-536-012 into J12. Plug the shields in the card guides adjacent to each board. Figure 2 shows the locations of components involved.

STANDARD RADIO

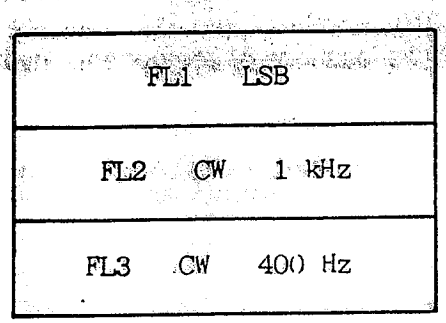


1A14
601076-536-010

MSR 5050 WITH FILTER OPTION



IF Filter #1
1A14
601076-536-013



IF Filter #2
1A12
601076-536-012

Figure 1
Filter Complements

ISB OPTION (610086-700)

4.1 GENERAL

The ISB Option adds a second simultaneous IF and audio signal path to the MSR 5050 receiver. This is accomplished by adding an IF Filter board (part number 601076-536-011) containing an LSB Filter and an Audio Squelch board (part number 601076-536-004 or -005) to AGC and demodulate the second channel. The MSR 5050 Mother board is altered by adding a jumper to condition the receiver program for ISB controls and by removing a jumper to reroute the LSB enable signal to IF Filter No. 2. The option is added to a receiver that has already been tested with a standard IF Filter board installed. Group -001 ISB Option is applied to a standard radio and contains and additional IF Filter board with an LSB Filter and second Audio Squelch board. Group -002 is applied to the radio in conjunction with IF Filter Option (which already includes both IF Filter Boards) and only requires an additional Audio Squelch board.

4.2 SPECIFICATIONS

Detection Mode:	Simultaneous USB and LSB
Controls:	ISB Mode Key - Pushbutton momentary key with LED to indicate activation.
	Monitor Keys - USB and LSB momentary pushbutton keys with LEDs to indicate activations. Causes corresponding speaker and meter indications.
Output:	Same specification on level, distortion, AGC, etc. as USB or LSB in the standard radio except USB and LSB occur simultaneously on J42 pins 22/20 and pins 18/16.
Sensitivity:	Same as USB or LSB - -113 dBm for 10 dB (S+N)/ N.

4.3 INSTALLATION

The MSR 5050 to be modified has previously been tested. Remove top cover and top shield. Remove jumper JP1 on the receiver Mother board. Add zero ohm resistor R11. Install Audio Squelch board No. 2 in J8. For -001 option install IF Filter No. 2 (part number 601076-536-011) in J12. Install a shield with each board added in the card guide slots adjacent to the circuit side of each board. All boards have been previously tested and adjusted. Reinstall top cover and top shield.

4.3.1 SENSITIVITY

Tune receiver to 11.347 MHz, ISB mode. Adjust generator to 11.348 MHz CW and record level to obtain 10 dB (S+N)/N on J42-22/20. Adjust generator to 11.346 MHz and record level to obtain 10 dB (S+N)/ N on J42-18/16.

4.3.2 OUTPUT LEVEL

Increase generator level to -7 dBm. ISB 600 ohm output level should be 0 dBm (adjustable by Audio Squelch No. 2 R64). Press LSB (monitor) and Audio (meter). Meter should indicate 0 dBm (adjust-

able by R63 at top of Display board). Monitor TP3 of Audio Squelch board No. 2 with a DC voltmeter. Decrease generator level to -47 dBm. Adjust R52 of that board for 8.5 + 0.5 VDC. With speaker switch ON and volume turned CW, a 1 kHz tone should be heard. Press RF (meter) key. Meter should indicate +100 dB uV (adjustable by Display board R66). Change generator to 11.368 MHz. Tone should again be heard. Press USB (monitor). Meter should indicate +100 dB uV (adjustable by Display board R64). Press AF (meter). Meter should indicate 0 dBm (adjustable by Display board R64). Standard 600 ohm output should be 0 dBm (adjustable by Audio Squelch board No. 1 R64).

Table 5.3A RECEIVER ASSEMBLIES

DESIGNATOR ASSEMBLY/SUBASSEMBLY	DESCRIPTION	PART NUMBER
1A1	Receiver Top Assembly	690024-000
1A1A1	Interface Board	601180-536-003
1A1A2	Mother Board	601212-536-001
1A1A3	Logic Board	601179-536-001
1A1A4	Chassis Assembly	600424-705-001
1A1A5	OCXO Assembly (option)	600173-378-001
1A1A6	FM Board (option)	601257-536-001
1A1A7	BFO Board (option)	601215-536-001
1A1A8	Audio Squelch Board (ISB Option)	601077-536-004,-005
1A1A9	Reference Board	601080-536-003
1A1A10	Audio Squelch Board	601077-536-004,-005
1A1A11	Minor Loop Board	601214-536-001
1A1A12	IF Filter Board (ISB option A) (Filter option)	601076-536-011 601076-536-012
1A1A13	Translator Loop Board	601083-536-001
1A1A14	IF Filter Board-Basic Receiver (Filter option)	601076-536-010 601076-536-013
1A1A15	Major Loop Board	601081-536-001
1A1A16	Mixer Board	601258-536-001
1A1A17	Current Loop/RS232 UART Board (Remote option)	601335-536-001
1A1A18	High Pass Filter Board	601086-536-001
1A1A19	Modem Board (FSK Remote option)	601181-536-001
1A1A19	FSK/Audio Modem Board (Voice plus Data Remote option)	601414-536-001
1A1A20	Low Pass Filter Board	601217-536-001
1A1A21	Front Panel Assembly, Grey	600066-539-001
1A1A21	Front Panel Assembly, Olive	600066-539-002
1A1A21A1	Display Board	601269-536-001
1A1A21A2	Keypad Board	601225-536-001
1A1A22	Rear Panel Assembly	600069-536-001
1A1A22A1	Power Supply Assembly	600423-705-001
1A1A23	Left Side Support Assembly	600500-706-001
1A1A24	Top Shield Assembly	600265-604-001
1A1A25	Top Cover Assembly	600706-612-001
1A1A34	Speaker Amplifier Board	601311-536-001

Table 5.4A RECEIVER ADJUSTMENTS

with 601258-536-001 Mixer Board
601076-536-010 IF Filter Board
601077-536-004 or -005 Audio Squelch Bd.

ASSEMBLY	ADJUSTMENTS AND PERFORMANCE
1A1A22A1 Power Supply Assembly	1) R18 (5 Volt Adj.): Measure dc voltage at rear panel J42-6. Adjust for 5.1 VDC.
1A1A16 Mixer Board (Put on extender for adjustment)	1) C35, C33, L14 (VHF IF Adj.): Frequency to 11.6 MHz, mode to USB. Apply 0.5 µV RF, adjust for maximum audio output (Adjustments only required after board repair. All adjustments preset at board test.)
1A1A14 IF Filter Board	1) JP2, JP3 (IF Gain): Position on E2-1,2 and E3-1,2 (away from board edge). 2) JP1 (TX ISB): Positioned down (on terminal 2 and 3) - transmit function only. 3) L20 (IF Bandpass tuning): Frequency to 11.6 MHz, USB. Apply 0.5 µV RF; adjust for maximum audio output. 4) R35 (IF Gain): Increase RF input to 7µV (-90 dBm). Adjust for 1.0 ±.2 v dBc at Audio Squelch board TP2 (or for a barely perceptable RF meter movement). 5) R7 (TX Gain): TX function only; no effect on receive.
1A1A10 Audio Squelch Board	POWER OFF. 1) R44 (S Meter): Adjust for 2k ohms from TP2 to R44 terminal 3 (top terminal). 2) R80 (squelch): Adjust for 2.7k ohms from E3 to ground. 3) R53 (DAGC Gain): Adjust for 100 ohms from R53 pin 3 (top terminal) to ground. POWER ON. Radio to 11.6 MHz, USB. Generator to 11.601 MHz, -47 dBm. 4) R52 (DAGC Offset): Adjust for 8.5 ± 0.5 VDC at TP3. Radio to 11.6 MHz, USB. Generator to 11.601 MHz and 13 dBm.

Table 5.4A RECEIVER ADJUSTMENTS (Cont.)

ASSEMBLY	ADJUSTMENTS AND PERFORMANCE
	5) Generator frequency to produce 1 kHz audio. Vary generator level from +13 dBm to -90 dBm. Audio level should change less than 3 dB. Adjust R53 CW if necessary. 6) R64 (600 ohm audio): Generator to 50 µV (-73 dBm). Adjust R64 for 0 dBm audio out into 600 ohms (J42 pin 22, 20). 7) JP1 (600 ohm MUTE): Normal position on E1 pin 1, 2 (top of board) does not allow muting or squelch of 600 ohm audio. Move to pins 2, 3 if desired.
1A1A21A1 Display Bd.	1) R65 (RF1 Meter Adj.): Same RF input but level to -7 dBm press "RF" meter switch. Adjust for full scale (+100 dBµV) meter indication. 2) R64 (AF1 Meter Adj.): Same input, press "AF" meter switch. Monitor STD 600 ohm output (rear panel 1A22J42 - pin 22/20) and adjust R64 for corresponding meter indication - normally 0 dBm. 3) R61 (Dimmer Adj.): Cover front panel photocell window to the left of the meter. Adjust R61 for barely discernable display intensity.
1A1 Interface Board	1) R42 (Tuning Center Adj.): Monitor TP1 (tuning voltage) should be 2.5 VDC. Adjust R42 to make TP2 voltage (tuning center) equal to TP1. 2) R48 (Scan Threshold): Monitor TP3 - receiver not in scan mode. Adjust R48 for .025 VDC. 3) R60 (Scan Delay): Adjust as desired during scan for .5 to 5 seconds.

3.1 INTERFACE BOARD, 1A1A1

The Interface Board is a plug-in PC board with dual 44 pin edge-card connections. It serves mainly as an interconnect between the MSR 5050 two front panel boards and the Mother board. Connection is made to the front panel boards via three ribbon cable connectors: J1 (26 pin) to the Display board, J2 (16 pin) to the Display board and J3 (34 pin) to the Keypad board. The Interface board is also used in the MSR 6406 Remote Control Unit.

3.1.1 KEYBOARD/DISPLAY CHIP

U9 is Keyboard/Display Chip 8279 which is used to perform key scanning and display refreshing. This chip interfaces with the microprocessor through common bus DBO thru DB7, write command WR, read command RD and clock signal ALE.

Information from the microprocessor is written into U9 during the write cycle if CS (U9-22) is low during this period. Information obtained is data if A0 is low during write cycle and is command if A0 is high during this period. Scan line SL0 through SL3 (U9-32) through 35 respectively) is a 4 bit encoded signal generated in U9 for key matrix and display scanning. All four bits are used for 16 digit display, but only the three LSBs are used for key matrix scanning.

Return line RL0 through RL7 (U9-38, 39, 1, 2, 5, 6, 7 and 8 respectively) are return signals from the key matrix. These lines are internally pulled up in U9 and can only be pulled low by a key closure.

B0, B1, B2, B3, A0, A1, A2 and A3 form an 8 bit word for the segments of LED display. Note that B0 is LSB. U9 is IRQ output. This pin is normally low and will go high when a key is closed and will go low again after the key code has been read.

U9-9 is reset input. U9 will be reset when this pin goes high.

3.1.2 D-TO-A CONVERTER CHIP

U8 is 8 bit DAC chip to perform A-to-D conversion for the receiver and D-to-A conversion for the remote control unit.

In A-to-D conversion, the converter output U12-7 is connected to a comparator U12D to compare with the incoming analog signal. The microprocessor will send out a stepping up digital signal starting from zero. As a result, the voltage in U12-7 will go up accordingly until its value equals the analog signal in U12-12. The comparator output U12-14 will change from high to low at this moment to interrupt the microprocessor chip to stop the stepping up action. The digital signal obtained at this moment is the equivalent digital value of the analog signal and the A-to-D conversion is completed.

In D-to-A conversion, the converter output U12-7 is connected to the meter circuit directly to drive the meter.

3.1.3 DECODERS

U1 decodes band informatin from the Logic board (bands A, B and C) and produces TTL low outputs (B1-8) to control the swtiching of filters in the Low Pass and High Pas Filter boards. U2 and U3 operate in parallel to decode filter bandwidth data (FLA, B, C) to produce TTL low outputs to control filter selection in the IF Filter boards (U3, pins 1-6) and to light LEDs in the Keypad initiating button (U2, pins 1-6). A decoded 5 (pin 6 of U2 and U3) will be used for FSK with a narrow offset filter in future options.

Pin 6 of U3 is bused to pin 4 to control the VNAR line, which corresponds to the physical position on the optional IF Filter board (FL3) where the FSK filter must be placed. Pin 6 of U2 is bussed to pin 3 to light the NAR key LED. U4 and U5 operate similarly to control mode selection lines (U5, pins 1-7) and the corresponding key button LED (U4, pins 1-7). The 74LS145 has open collector outputs to allow pull-ups to 9 volts for control and to 5 volts for LEDs. U10C produces a TTL low (via Q1) only when both lines P1-10 and P1-11 are high. U18B and U17 are used as LED drivers.

3.1.4 FREQUENCY SCAN CIRCUITS

A variable rate pulse is generated on either P2-18 or 19 as the DC voltage on J2-4 goes above or below 2.5 VDC. U7A, B and CR9 and 10 form an absolute value detector which produces an output DC voltage proportinal to the difference between 2.5 volts and the input voltage. The output pulls down the base of Q2 via R35 or R33/CR13 to vary the current in Q2. The current in Q2 controls the charge rate of C24 and thus the pulse output frequency of the timer (U13A). U13B acts as a constant pulse width inverter. U7C and D are biased to produce +5 volts output when the input is slightly above 2.5 volts (U7D) or slightly below 2.5 volts (U7C).
The outputs are gated through U10A (up control) or U10B (down control) with the slight difference in bias assuring a dead zone where neither U10A nor B are gated on.

3.1.5 METER CIRCUITS

Audio inputs on P1-4 and 12 are rectified (CR7 and CR8) and peak detected (U11A, B and CR19, 21) to produce DC outputs proportional to audio level to drive a meter.

3.1.6 CHANNEL SCAN CIRCUITS

The scan circuitry is enabled by a TTL high on P2-6 which allows the scan oscillator U12A to start (by grounding C28 via U18A) and arms the scan delay monostable U19A by removing the TTL low on the clear input, pin 3. U12A oscillates at a rate determined by C28 and a 100k variable resistor on the Keypad board accessable from the front panel. The output is differentiated and limited to 5 volts peak to drive the Logic board microprocessor (via P2-14). The microprocessor will iniate a channel change upon receiving the scan oscillator pulse unless a TTL high is produced from the scan delay monostable U19A-6 (via P2-18). If a high is sensed, the microprocessor will change channels as soon as the scan delay output goes low. When the channel changes, a narrow TTL low pulse ($\approx$ 2 Msec) is put on P2-6 which triggers a signal inhibit one-shot U19-B (pin 11) producing a 100 Msec (C35, R62) TTL high pulse (pin 10). This raises the trigger threshold (set by R48) on signal detector U12C (pin 10), thus prohibiting triggering on transient signals during channel change.

Audio signals coming into comparator U12C-9 above a threshold voltage (set by R48) will produce negative-going pulses to trigger the scan delay monostable, U19 (pin 4). The scan delay is variable by R60 in conjunction with C34 from .5 to 5 seconds. When U19A is triggered, a TTL low signal is put out from U19-7 (Q) to P2-16 to indicate signal presence.

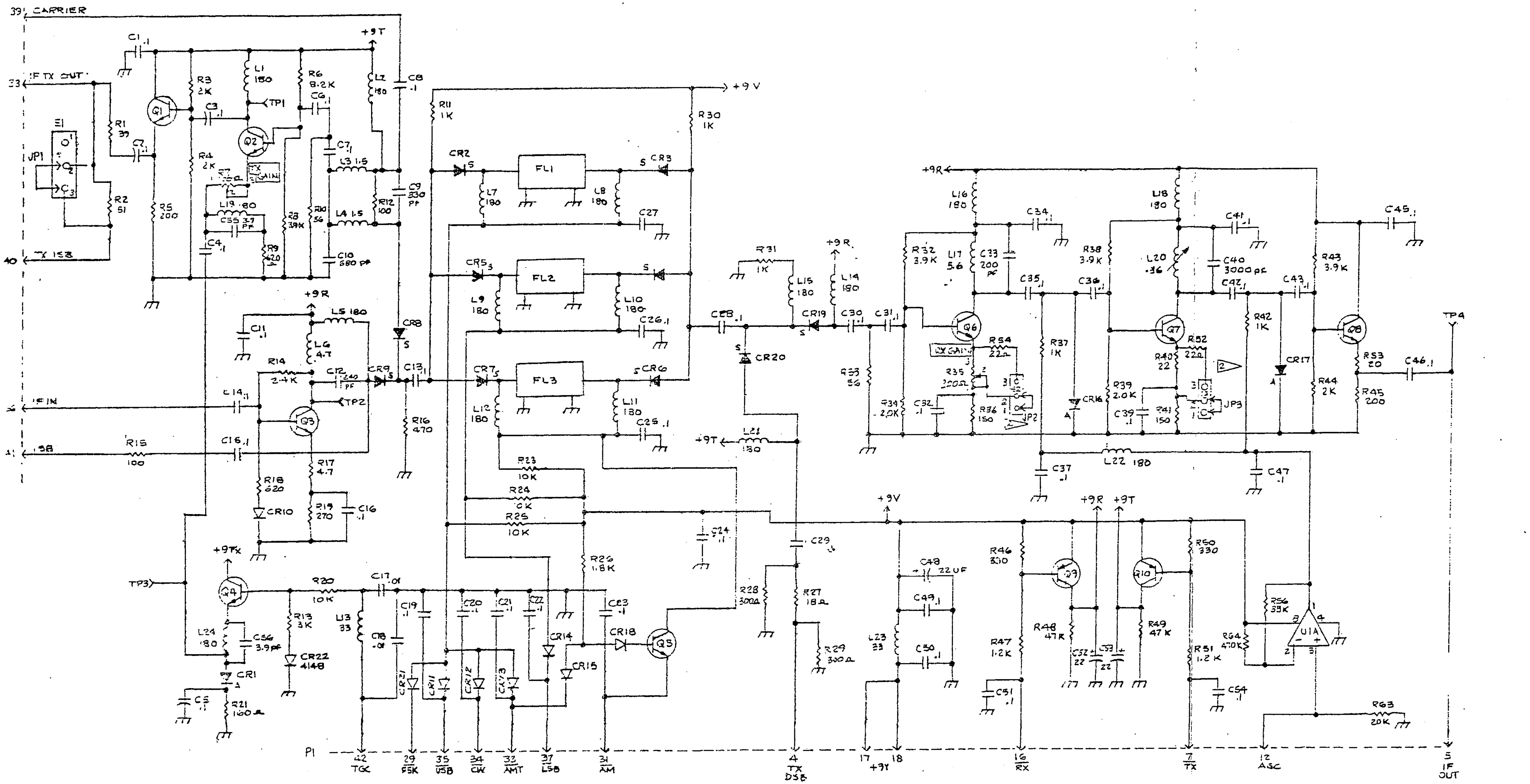
With jumper JP2 between E2-2 and 3, U19 cannot be retriggered during the scan delay period. At the end of the delay period, the rising pulse from Q (U19-7) triggers the signal inhibit monostable at U19-12 to prevent retrigger until the channel is changed. The same rising edge of Q triggers the scan oscillator via C36 to ensure that the scan dwell for the next channel will be a full period.

INTERFACE BOARD (601180-536-003)

SYMBOL	DESCRIPTION	PART NUMBER
C24	Cap., .33 µf, 35V	600202-314-004
C12,13	Cap., 10 µf, 25V	600202-314-018
C5,27	Cap., .01 µf, 400V	600204-314-001
C1-4,6,9-11,23,26	Cap., .1 µf, 50V	600272-314-001
C36-39		
C25	Cap., .001 µf, 50V	600272-314-008
C35	Cap., 3.3 µf, 50V	600297-314-008
C7	Cap., 22 µf, 25V	600297-314-016
C8,28	Cap., 100 µf, 25V	600297-314-032
C34	Cap., 220 µf, 10V	600297-314-037
CR11,14-18,25	Diode, 1N270	600052-410-001
CR3,5-10,19-24, 26-29	Diode, 1N4148	600109-410-001
CR30	Diode, 1N4148	600109-410-001
CR13	Diode, 1N4746A	600002-411-001
CR1,2	Diode, Zener, 1N4371A, 2.7V	600002-411-030
CR12	Diode, 1N4739A, 9.1V	600006-411-012
E1,2	Header	600198-608-005
J2	Header, 800-588	600174-608-003
J1	Header, 26 Pin	600174-608-005
J3	Header, 34 Pin	600174-608-006
JP1,2	Conn., Jumper	600190-608-001
Q1	Transistor, 2N2222A	600080-413-001
Q2	Transistor, 2n2907A	600154-413-001
R73	Resistor, 1/4W, 5%	600000-341-075
R58	Resistor, 100Ω, 1/4W, 5%	610004-341-075
R1,45,59	Resistor, 1k, 1/4W, 5%	610014-341-075
R3,4,7-11,15,17-20,44,67,32,64, 71,72	Resistor, 10k, 1/4W, 5%	610024-341-075
R27,46	Resistor, 100k, 1/4W, 5%	610034-341-075

INTERFACE BOARD (601180-536-003)

SYMBOL	DESCRIPTION	PART NUMBER
R28	Resistor, 1k, 1/4W, 5%	611024-341-075
R31	Resistor, 120k, 1/4W, 5%	612034-341-075
R30	Resistor, 150k, 1/4W, 5%	615034-341-075
R26	Resistor, 180k, 1/4W, 5%	618034-341-075
R68,43	Resistor, 20k, 1/4W, 5%	620024-341-075
R36,63,40,41	Resistor, 220Ω, 1/4W, 5%	622004-341-075
R6,61,69,14	Resistor, 2.2k, 1/4W, 5%	622014-341-075
R25	Resistor, 2.2M, 1/4W	622044-341-075
R62	Resistor, 27k, 1/4W, 5%	627024-341-075
R2	Resistor, 33k, 1/4W, 5%	633024-341-075
R12,13	Resistor, 39k, 1/4W, 5%	639024-341-075
R16,70	Resistor, 470k, 1/4W, 5%	647004-341-075
R5,33,34,66	Resistor, 4.7k, 1/4W, 5%	647014-341-075
R37	Resistor, 47k, 1/4W, 5%	647024-341-075
R65	Resistor, 470Ω, 1/4W, 5%	647034-341-075
R39	Resistor, 5.1k, 1/4W, 5%	651014-341-075
R38	Resistor, 51Ω, 1/4W, 5%	651094-341-075
R35	Resistor, 62k, 1/4W, 5%	662024-341-075
R48,42	Potentiometer	600089-360-010
R60	Potentiometer	600089-360-014
U6	IC NE555, Timer	600074-415-001
U11,20	IC LM358, Op Amp LP Dual	600150-415-001
U7,12	IC LM324, Op Amp 741 Quad	600171-415-001
U17,18	IC 74LS33, Nor, 2-In, Quad	600219-415-001
U13	IC LM556, Dual Timer	600237-415-001
U10	IC 74LS08 and 2-In Quad	600271-415-001
U9	IC 8279, Keybd/Disp	600507-415-101
U1-5	IC 74LS145, BCD to Deci	600528-415-001
U8	IC DAC083LCN, D-A Conv	600605-415-001
U19	IC 74HC4538	700108-415-001
XU8	IC Socket	600119-419-020
XU9	IC Socket	600119-419-040
Z1,2	Res. Network, 4.7k x 7	600201-537-001



NOTES:

1. JP1 BETWEEN E1-2 AND E1-3 FOR NORMAL OPERATION, BUT FOR A MSR-6700 WITH ISB PUT JP1 BETWEEN E1-1 AND E1-2.
2. PLACE JP2 AND JP3 BETWEEN PINS 1 AND 2 FOR VOICE MODE. CONNECT JP2 AND JP3 BETWEEN PINS 2 AND 3 FOR DATA MODE.

CAPACITORS IN UF
RESISTORS 1/4W 5%

IC = LM358

GND PINS 1,2,23,24,43,44

CHOKES IN µH 1/4W
TRANSISTORS 2N3904 NPN 2N3906 PNP
DIODES = 1N4148
S = HP5082-3188
A = HP5082-3080

NOT USED	LAST USED
R27,55 57-62	L24
C28	Q10
C44	R64
	C56
	CR22
	JP3
	E3

IF Filter Board Schematic

4.1 IF FILTER BOARD

The IF Filter board contains the three selectable 5 MHz information filters and amplifiers used in both receive and transmit operation. These filters are:

- FL1, upper-sideband operation; also used for CW, FSK, AME (transmit) and A3A (transmit).

- FL2, lower sideband operation

- FL3, AM operation (receive)

The appropriate filter is selected by diode steering via mode information from the Interface board. During the receive mode, a 5 MHz IF signal from the High Level Mixer board is passed through the appropriate IF filter and further amplified in three stages. The gain is adjustable by jumpers to produce a 7 μV AGC threshold (for voice reception) or 1.4 μV threshold (for data reception). An AGC voltage from the Audio Squelch board controls the gain of the amplifiers to maintain a constant IF output over a large range of input levels.

In transmit operation, a 5 MHz double-sideband signal from the Transmit Modu-lator board is applied. The appropriate filter (FL1 or FL2) removes the unwanted sideband. A hybrid combiner adds a controlled level of 5 MHz carrier to the signal in AME and A3A transmit modes. The signal is then routed to the output through an amplifier with gain controlled by a TGC (Transmit Gain Control) voltage from the Transmit Modulator board.

4.1.1 DETAILED DESCRIPTION

4.1.1.1 Filter Selection

The filters are selected by placing a ground (logic 0) on certain pins on the board connector. FL1 is used to receive and transmit USB, CW and FSK, and to transmit AME and A3A. Since the frequency is inverted in the mixer, the USB filter passband is actually on the lower side of 5 MHz.

When USB is selected, a ground is placed on pin 35 of P1. This action causes AC current flow from the +9V bus through R11, CR2, L7, and CR11. The resulting low resistance of pin diode CR2 creates a signal path from L13 to FL1 input. The high impedance of R11 and L7 prevent loading the signal. The other filter selector diodes, CR5 and CR7 are back-biased by the 9 volts supplied through pull-up resistors R23 and R24, and the near-zero volts at their anodes caused by pulling in CR2.

The filter output is similarly selected by CR3 with current from +9V through R30, CR3 and L8, to the same ground at pin 35. FL1 is also selected by the same action with grounds on pin 29 ($\overline{\text{FSK}}$) through CR21, pin 34 ($\overline{\text{CW}}$) through CR12, pin 33 (AMT) through CR13.

FL2 (LSB) is selected by a similar process with a ground on pin 37, causing current flow from +9V through R11, CR5, L9, and CR14 (to connect the input) and current flow through R30, CR4, L10, and C14 (to connect the outputs).

FL3 is selected for receive AM operation by a ground on pin 31, which biases Q5 on (the base being pulled to +9 VDC through R26), causing current flow through the input and output selector diodes CR7 and CR6. FL3 is prevented from being selected in AMT (transmit AM operation) by the ground at pin 33 which biases Q5 off through CR15.

4.1.1.2 Receive Path

The 5 MHz receive input from the Mixer is on pin 36. Q3 provides 22 dB gain with a 50 ohm input and output impedance.

The 50 ohm input is controlled by the series/shunt feedback of R17/R14. L6 and C12 match the 400 ohm collector impedance to 50 ohms. The gain is controlled by the ratio of the collector load to R17. Q3 is biased for 6 mA collector current by R19 for an output third order IM intercept point of +19 dBm, allowing less than -40 dB inband IM distortion at IF inputs up to -28 dBm.

The amplified signal from Q3 passes through CR9 and C13 to the selected filter. CR9 is biased "ON" by the current through R16 and L5 from the "+9R" voltage bus, which is activated in the receive mode by Q9. The voltage developed across R16 back-biases CR8 to prevent loading from the transmit circuitry.

The output of the filter is similarly routed through C28 and CR19 with CR19 biased on by current through L14, L15, and C31 from the "+9R" bus. CR20 is biased off by the voltage developed across R31. C30 and C31 couple the 5 MHz signal to Q6 which provides 31 dB voltage gain into a typical 300 ohm load (17 dB power gain). The 56 ohm R33, shunts the high input impedance of Q6, providing an accurate 50 ohm load for the filters. A variable resistor, R3, in the Q6 emitter, adjusts the gain of Q6 to overcome tolerances in the receive signal path and establishes a fixed end-to-end board gain. This adjustment directly effects the AGC threshold for the receiver. Jumper JP2 (and JP3 for Q7) shunts a 22 ohm resistor across the emitter resistor R35 (R40 for Q7) increasing the stage gain by about 6 dB, which reduces the receiver AGC threshold from -90 to -104 dBm. Q6 gain is proportional to the ratio of the load impedance of about 300 ohms (deter-mined mainly by the parallel impedance of R37, R38, R39, the input impedance of Q7 and the off resistance of CR16) to the unbypassed emitter resistance.The gain is reduced by 30 dB in response to an AGC voltage from pin 12, by current through pin diode CR16 which reduces the load resistance of Q6. The response of Q6 is broadly tuned to 5 MHz (loaded Q of 2 by L17 and C33).

The signal is further amplified by Q7 in a nearly identical circuit with 17 dB gain. The output is sharply tuned (loaded Q of 50) by C40 and variable inductor L20 to reduce the broadband noise in the signal path.

The collector load is 500 ohms for this stage. Q8 is an emitter follower which produces a low inpedance output to the following Audio Squelch board through pin 5. A 20 ohm emitter resistor R53, limits the current gain for low impedance output loads which may compromise stability.

U1 is a voltage follower which passes inputs at pin 12 to a 0-6 volt output to pin diode (CR16, CR17) bias resistors (R37, R42), producing up to 6 mA current in each diode. This provides AGC gain cuts of 30 dB for each diode. U1 input is offset by R64.

The overall gain is 55 dB in voice mode, which produces a 7 μV AGC threshold in the radio with a -30 dBm Audio Squelch board AGC input threshold and 67 dB gain in data mode (JP2 and JP3 positioned E2, pin 1-2 and E3, pin 1-2), producing a 1.4 μV AGC threshold- adjustable in both cases by R35.

The AGC gain cut is 60 dB with an AGC voltage input voltage of 8 VDC. The in-band IM rejection is greater than 40 dB at inputs up to -31 dBm. The noise figure is about 4 dB.

4.1.1.3 Transmit Path

The double sideband input to the IF Filter board on pin 4 from the Transmit Modu-lator is attenuated 3 dB by R27, R28, R29 and applied to the selected filter through C29 and CR20. CR20 is biased "ON" by current through L21, L15, and R31 from the "+9T" buss which is activated by Q10 in transmit mode. The USB or LSB signal emerging from the filter is passed through C13 and CR8 (by bias current from "+9T" through L2, L3, L4, and R16) to a 3 dB combiner circuit tuned at 5 MHz. The combiner, which adds a carrier (pin 39) to the SSB signal in AME or A3A mode, is formed by L3, L4, C9, C10, and R12.

The output of the combiner goes through C7 and C6 to the base of Q2 with R10 imposing a 56 ohm termination to the combiner and consequently, to the filters. Q2 is configured as a common emitter amplifier with maximum gain determined by the ratio of the collector load of 1k (R3/R4 in parallel) and the unbypassed emitter resistor R9, which is adjustable to maintain a precise transmit gain. The gain is varied by the resistance of pin diode CR1 in the emitter circuit in series with R9 in response to TGC voltage from 2 to 6 VDC at pin 42.

Parallel traps L19/C55 and L24/C56 are tuned to 5 MHz to remove parasitic loading in the emitter circuit to maximize the TGC gain cut to greater than 32 dB. R13 and R20, in conjunction with the diode junction voltages of CR1, Q4 vs. CR21, delay the TGC action until approximately 2 VDC.

Q1 is an emitter follower producing a 50 ohm output impedance at pin 38 (and pin 40). When used in the MSR 6700 in ISB, where two IF Filter boards are paralleled at pin 40, JP1 is connected to E1, pin 1 to 2. This produces a 100 ohm output for each board with a resulting 50 ohm source impedance to the following Mixer board.

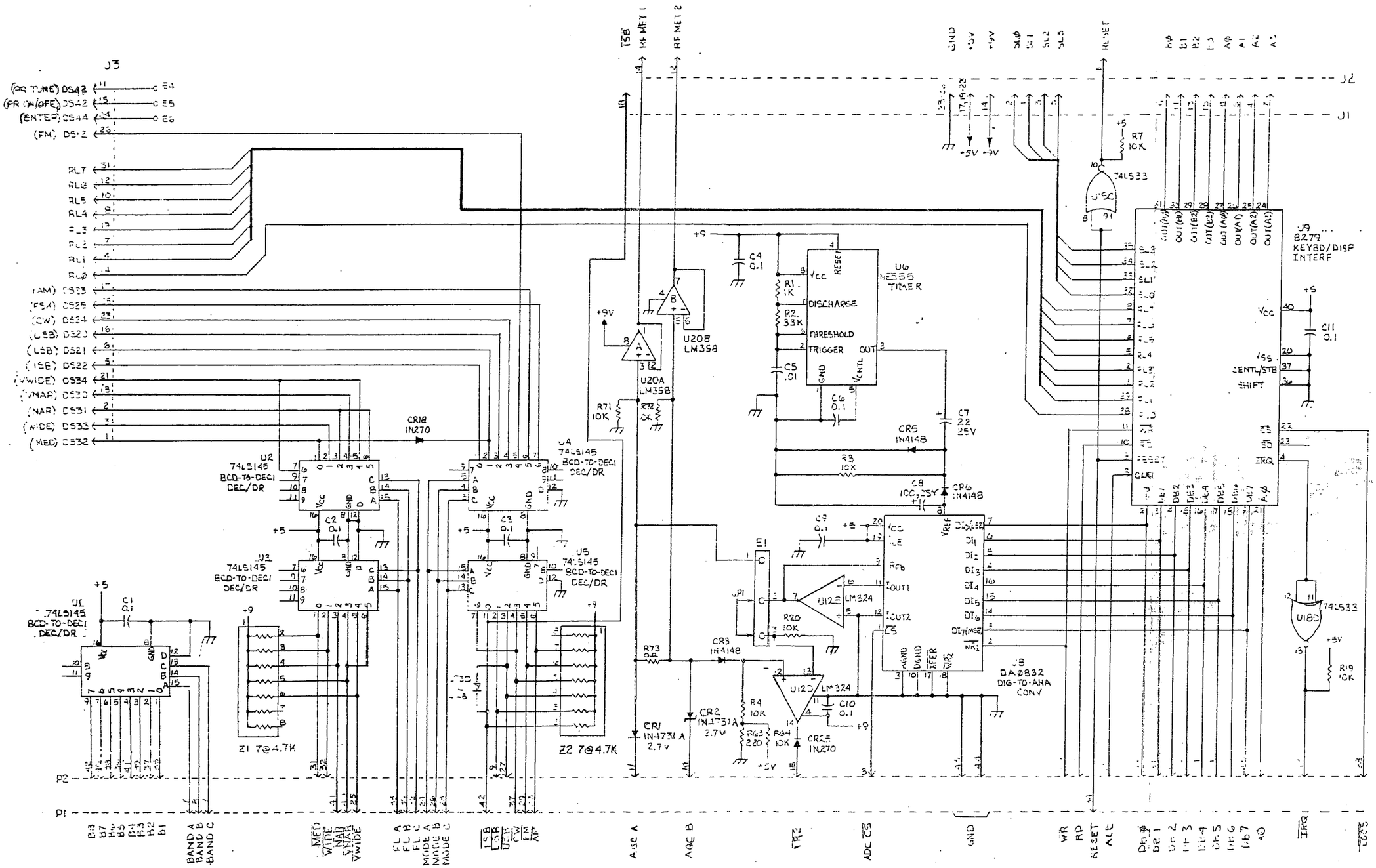
With a +5.5 VDC TGC input at pin 42, the overall SSB transmit gain from pin 4 to pin 38 or pin 40 is +6 dB and carrier gain from pin 39 to pin 38 or 40 is +13 dB. Both gains are reduced by 32 dB by a TGC input at pin 42 from +5.5 to 2 VDC. Third order IM products are down greater than 40 dB with DSB inputs as high as 10 dBm.

IF FILTER BOARD
(601076-536-010)

SYMBOL	DESCRIPTION	PART NUMBER
C17,18	Cap., 0.01 µf, 100V	600302-314-007
C1-8,11,13-16,19-32,34-37,39,41-43,45-47,49-51,54	Cap., 0.1 µf, 63V	600302-314-013
C55,56	Cap., 3.9 pf	600265-314-008
C9	Cap., 330 pf	600293-314-331
C10	Cap., 680 pf	600293-314-681
C12	Cap., 240 pf	600293-314-241
C33	Cap., 200 pf	600293-314-201
C40	Cap., 3000 pf	600265-314-026
C48,52,53	Cap., 22 µf, 25V	600297-314-016
CR1,16,17	Diode, HP3080	600156-410-001
CR2-9,19,20	Diode, HP3188	600144-410-001
CR10-14,18,21,22	Diode, 1N4148	600109-410-001
CR15	Diode, 1N270	600052-410-001
E1,2,3	Header, 3 Pin	600198-608-005
JP1,2,3	Jumper	600190-608-001
L1,2,5,7-12,14-16,18,19,21,22,24	Choke, 180 µH	600125-376-022
L3,4	Choke, 1.5 µH	600125-376-033
L6	Choke, 4.7 µH	600125-376-030
L17	Choke, 5.6 µH	600125-376-043
L13,23	Choke, 33 µH	600125-376-007
L20	Coil, Var., 0.36 µH	600247-376-001
Q1-8	Trans., 2N3904-18	600229-413-003
Q9,10	Trans., 2N3906-18	600116-413-002

IF FILTER BOARD
(601076-536-010)

SYMBOL	DESCRIPTION	PART NUMBER
R7	Pot, 100Ω	600066-360-004
R35	Pot, 200Ω	600066-360-005
R1	Res., 39Ω, 1/4W, 5%	639094-341-075
R2	Res., 51Ω, 1/4W, 5%	651094-341-075
R3,4,34,39,44	Res., 2k, 1/4W, 5%	620014-341-075
R5,45	Res., 200Ω, 1/4W, 5%	620004-341-075
R6	Res., 8.2k, 1/4W, 5%	682014-341-075
R8,32,38,43	Res., 3.9k, 1/4W, 5%	639014-341-075
R28,29	Res., 300Ω, 1/4W, 5%	630004-341-075
R10,33	Res., 56Ω, 1/4W, 5%	656094-341-075
R11,30,31,37,42	Res., 1k, 1/4W, 5%	610014-341-075
R12,15	Res., 100Ω, 1/4W, 5%	610004-341-075
R14	Res., 2.4k, 1/4W, 5%	624014-341-075
R16	Res., 470Ω, 1/4W, 5%	647004-341-075
R17	Res., 4.7Ω, 1/4W, 5%	647084-341-075
R9,18	Res., 620Ω, 1/4W, 5%	662004-341-075
R19	Res., 270Ω, 1/4W, 5%	627004-341-075
R13	Res., 3k, 1/4W, 5%	630014-341-075
R21	Res., 160Ω, 1/4W, 5%	616004-341-075
R26	Res., 1.8k, 1/4W, 5%	618014-341-075
R20,23-25	Res., 10k, 1/4W, 5%	610024-341-075
R27	Res., 18Ω, 1/4W, 5%	618094-341-075
R36,41	Res., 150Ω, 1/4W, 5%	615004-341-075
R46,50	Res., 330Ω, 1/4W, 5%	633004-341-075
R47,51	Res., 1.2k, 1/4W, 5%	612014-341-075
R48,49	Res., 47k, 1/4W, 5%	647024-341-075
R53	Res., 20Ω, 1/4W, 5%	620094-341-075
R56	Res., 33k, 1/4W, 5%	633024-341-075
R63	Res., 20k, 1/4W, 5%	620024-341-075
R40,52,54	Res., 22Ω, 1/4W, 5%	622094-341-075
R64	Res., 470k, 1/4W, 5%	647034-341-075
U1	IC, LM358	600150-415-001



GRP:- 003

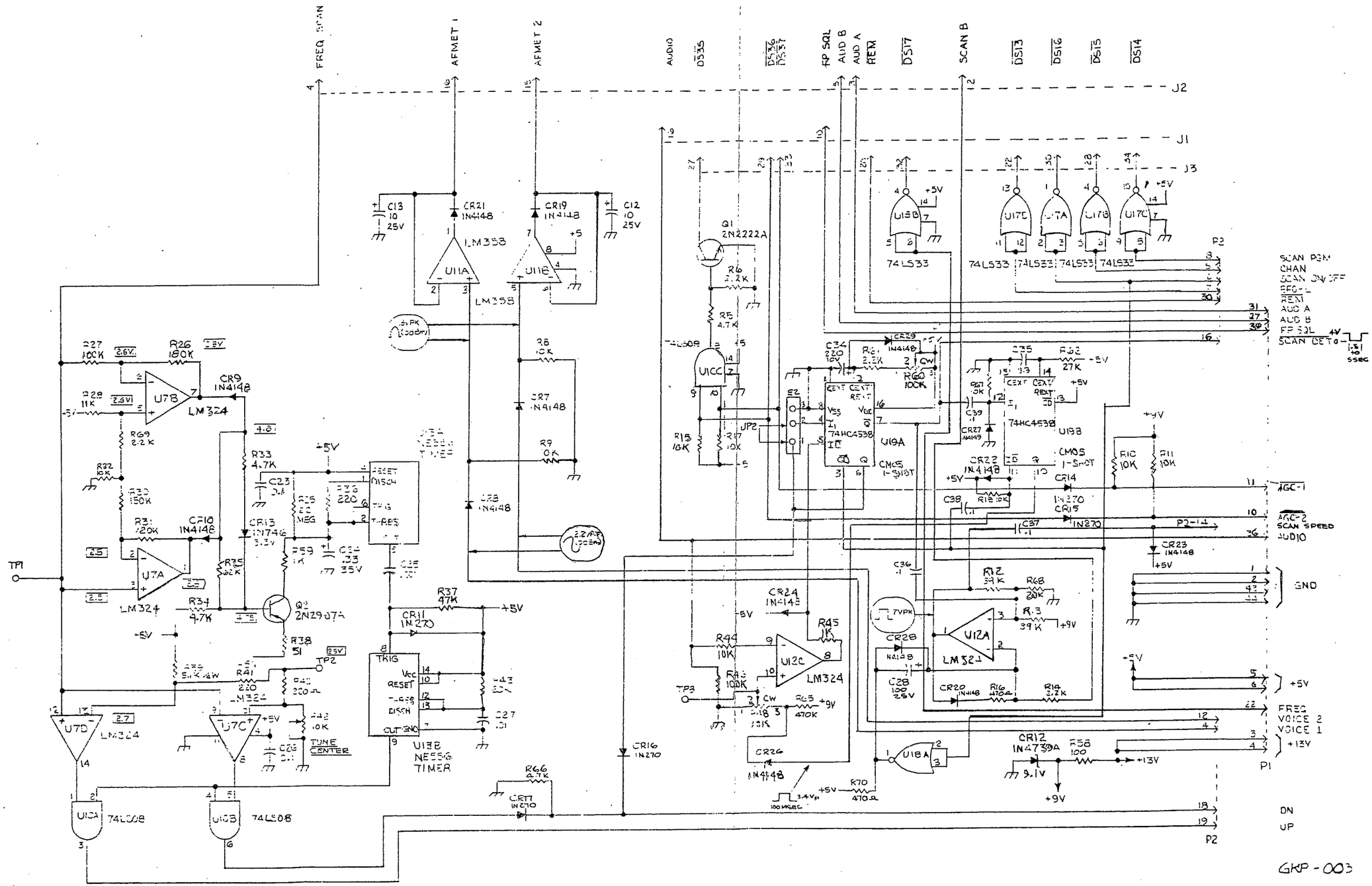
NOTES:

1. ALL CAPACITORS ARE IN MICROFARADS, ALL RESISTORS ARE IN OHMS, 1/4 WATT, 5% TOLERANCE, UNLESS OTHERWISE SPECIFIED.
2. CONNECT E1-2 TO E1-3 WITH JP1 WHEN USED IN MSR505C. CONNECT E1-2 TO E1-1 WITH JP1 WHEN USED IN MSR6406.

SPARE GATES

LAST REF DESIGNATED
C39, CR28, J3, P2
R73, Q3, U20, Z2
E2, JP2

Interface Board Schematic (Sheet 1 of 2)



DC VOLTS WITH 2.5VDC AT J2-4

AC VOLTS

Interface Board Schematic
(Sheet 2 of 2)

5.1 AUDIO SQUELCH BOARD

The Audio Squelch board is used in receive mode only. This board accepts the 5 MHz IF output from the IF Filter board and performs the final detector function to convert the intermediate frequency signal into usable audio intelligence. A product detector is used in SSB, CW, FSK, and Data modes while an envelope detector is used in the AM mode. Two separate audio outputs are provided: One ultimately converted to a balanced 600 ohm rear panel output via the Input/Output Interface board and one converted to a front panel speaker/ phone audio via the Speaker Driver board with level adjusted by the front panel volume control.

Located on this board are an input IF amplifier, envelope detector, AGC circuit, delayed AGC circuit, product detector, 3rd LO amplifier, 600 ohm audio amplifier circuit, speaker/sidetone audio circuit, and squelch circuits.

The AGC has a fast attack and front panel selectable fast, medium, or slow decay times. The squelch circuit is a combination of syllabic (responding to frequencies less than 500 Hz modulated at rates less than 5 Hz) with a front panel adjustable carrier squelch. A jumper JP1 positioned on E1 pins 2 and 3 will allow the 600 ohm audio as well as the speaker audio to be squelched.

5.1.1 DETAILED DESCRIPTION

5.1.1.1 Input IF Amplifier and Envelope Detector

5 MHz input signals from the IF Amplifier, at pin 5, at a level of 20 mV P-P will activate the AGC circuits. Q1 is a common emitter amplifier with 36 dB voltage gain to the gate of Q2. The collector load is 650 ohms by R8 in parallel with the loading, due to C5 and its 50 ohm termination due to R5, R6, etc. C5 matches the high impedance to the 50 ohm operating impedance of a double balanced diode mixer into R5, R6, and R7, providing 3 dB attenuation and stabilizing impedance to the product detector J1, reducing the 5 MHz IF signal to about -10 dBm. Q2 is an FET source follower buffer amplifier which drives the envelope detector Q3. Q2 source resistor R9 provides bias current for CR1 through L4, which provides a near optimum offset bias voltage at the base of Q3, for a wide detector dynamic range with temperature compensation. The detected envelope with carrier rejected by C9 is routed through C20 to an analog SPDT section of U2, which selects either the product detector output in SSB, FSK, and CW or the envelope detector signal in AM. The envelope signal is also applied to the AGC circuit at U1 pin 3,10.

5.1.1.2 Product Detector and LO Amplifier

The 5 MHz third LO signal for the product detector is received on pin 12 at a 50 ohm reference -15 dBm level. Q4 provides 24 dB gain to produce a +4 dBm LO drive via matching capacitor C13 to the product detector J1 at pin 8. The 5 MHz IF signal input to the product detector is received via the 3 dB attenuator (R5, R6, and R7) at a level of --10 dBm at pin 1. The detected output at 62 mV RMS is applied to the analog switch U2 at pin 12 with the 5 MHz carrier and image frequencies rejected by C11. The LO and IF levels at the mixer maintain IM distortion less than -40 dBc.

5.1.1.3 600 Ohm Audio and Speaker Audio

The selected AM or product detector signal from U2A, pin 14 is amplified by 3.3 to 200 mV RMS by the ratio of R32 to R31. This audio level from SSB (100% modulated) is the same as that from 100% AM modulated signals. The AC ground reference for U4A is a 4.5 volt bus created by U5A and voltage divider R70, R71 from +9V. Inputs and outputs of analog switches U2A, B, and C are also referenced

to the same bus to eliminate transient outputs in the audio during switching. The 600 ohm audio signal is routed through the MUTE/SQUELCH switch U2, pin 1 to 15 unless bypassed by JP1 from E1, pin 1 to 2. Variable resistor R64 attenuates the signal to the 600 ohm line amplifier U4B/Q10. The gain of the amplifier is determined by feedback resistors R60 and R61 with Q10 increasing the output current drive to produce +10 dBm (6.9V P-P) at T1 output when loaded with 600 ohms at board connector pins 14 and 6.

The peak current drive is established by R62, which produces a quiescent current of 25 mA due to the 4.5 VDC bias at Q10 collector. The bias voltage results from the 4.5V buss at U4B, pin 6 and the closed loop DC voltage gain of 1. The 600 ohm output impedance is established by feedback resistor R63 at T1 centertop to ground (150 ohms from T1, pin 4 to pin 5). The ratio of 150 ohms to R63 is the same as that of the primary gain resistors R60 to R61. When the secondary of T1 is not loaded, the voltage gain is determined only by R60 and R61. When loaded by 600 ohms, the reflected impedance between T1, pin 4 and 5 is 150 ohms. This produces a feedback factor with R63 equal to that of R60 and R61, which reduces the gain and consequently the output voltage by a factor of 2 - - evidence of a matched 600 ohm source impedance. In the MSR 5050, the balanced 600 ohm output produced in the Input/ Output Interface board from the single ended 150 ohm output T1, pin 6 at Audio Squelch board, pin 4. The voltage gain of the amplifier circuit is 29 dB to a 600 ohm load at pin 6/14 or to an open circuit load (as for the MSR 5050) at pin 4. This produces 2.45V RMS (40 dBm into 600 ohms) with 86 mV RMS input from R64, which allows a 7 dB gain margin from the 200 mV RMS available at R64.

The speaker audio signal goes through analog switch U2, pin 3 to 4 with no bypass jumper. The signal is reduced in amplifier U4C to 150 mV RMS at board pin 3 by the ratio of R67 to R65. This output is amplified to a speaker/phone front panel output in the Speaker Driver board with level control by the front panel volume control. A CW sidetone signal from the Transmit Modulator at board pin 27. The peak current drive is established by R62, which produces a quiescent current of 25 mA due to the 4.5 VDC bias at Q10 collector. The bias voltage results from the 4.5V bus at U4B, pin 6 and the closed loop DC voltage gain of 1. The 600 ohm output impedance is established by feedback resistor R63 at T1 centertop to ground (150 ohms from T1, pin 4 to pin 5). The ratio of 150 ohms to R63 is the same as that of the primary gain resistors R60 to R61. When the secondary of T1 is not loaded, the voltage gain is determined only by R60 and R61. When loaded by 600 ohms, the reflected impedance between T1, pin 4 and 5 is 150 ohms. This produces a feedback factor with R63 equal to that of R60 and R61, which reduces the gain and consequently the output voltage by a factor of 2 - - evidence of a matched 600 ohm source impedance.

In the MSR 5050, the balanced 600 ohm output produced in the Input/Output Interface board from the single ended 150 ohm output T1, pin 6 at Audio Squelch board pin 4. The voltage gain of the amplifier circuit is 29 dB to a 600 ohm load at pin 6/14 or to an open circuit load (as for the MSR 5050) at pin 4. This produces 2.45V RMS (40 dBm into 600 ohms) with 86 mV RMS input from R64, which allows a 7 dB gain margin from the 200 mV RMS available at R64.

5.1.1.4 Squelch Circuits

The syllabic squelch circuit is basically a pulse count discriminator and integrator which produces a gating output for slowly changing (less than 5 Hz rate) frequency content of the audio signal. The gating output has a fast attack (50 milliseconds) and long hang-time (2 seconds).

The audio signal is first amplified (U6B, pin 5) by 1000 (R87/R88) in U6B, and squared in U6C to produce a square wave input at U7A, pin 1 for signals downto receiver noise levels. U7A and U7B form a monostable multivibrator with an output pulse width of 0.5 milliseconds and a saturated output level of 4 volts. A differentiator (C49, C50, R86, and R85) and integrator (R84, R83, C51, and C52) produce

a DC voltage output proportional to the average frequency of the audio signal. U6A is an integrator with a gain of 10, determined by R81/R82 and a time constant of 73 milliseconds (R81, C45). This reduces output due to fast frequency changes greater than 5 Hz. R80 is normally set to attenuate the signal by .27, but may be adjusted in unusually noisy environments to prevent squelch breaks by noise. U5D is an absolute value amplifier which produces a negative output when the peak voltage changes from R80 exceed the forward voltage drop of either CR17 or CR18. The one-shot voltage formed by U7D, U7C is triggered through CR16 and resets in about 2 seconds (unless retriggered) due to the time constant C43, R75.

The resultant +9 VDC positive output from U7C through CR15, forces comparator U5B input (U5B, pin 5) high, which in turn enables the 600 ohm audio gate U2B and the speaker audio gate U2C by +9V on U2, pin 9 and 10.

The squelch gates are also enabled through comparator U5B by another comparator, U5C, which is driven by the front panel squelch control through attenuator R73/R72. With the squelch control fully counterclockwise, the wiper outputs +9 VDC to Audio Squelch board pin 10 and is attenuated to 4.9 VDC, which exceeds the 4.5V comparator reference voltage at U5C, pin 9, thus enabling the squelch gate. With the squelch control about 25° clockwise, the squelch gate may be enabled only by the syllabic circuit, or by a carrier squelch controlled by FET Q8 from the AGC voltage at U1B, pin 7. The source of Q8 is fed to R45/R46, which is driven from 4.5 to 9V by the AGC circuit in response to increasing antenna signal levels. When the source of Q8 exceeds the gate voltage as set by the front panel squelch pot by an amount equal to the pinch-off voltage (about 3 volts), Q8 turns on and produces a voltage across R56. When this voltage exceeds U5B reference voltage of 4.5 volts, the squelch gate is enabled. Varying the squelch control clockwise (reducing the voltage at Q8 gate) increases the antenna signal level required to enable the squelch gate.

5.1.1.5 AGC Circuits

U1A is a X50 amplifier/peak detector which amplifies signals from Q3 that exceed a reference voltage of .24 VDC (set by R25/R26). The gain is set by R23/R24. The AGC attack time is limited by the charging time of C23 through R95 and R22 to less than 10 milliseconds.

CR24 bypasses R96 to reduce the attack time for large signal changes. The decay time is determined by the discharge time constant of C23 through R23 for 1.5 seconds in slow AGC through R39 for 200 milliseconds in medium AGC, and through R38 for less than 50 milliseconds in fast AGC.

U1C is identical to U1A, but with a gain of 200 (by R28/R27) and a fast charge/ discharge time. The outputs of both amplifiers are compared in U1D. The output of U1C is normally higher than U1A; U1D output is low. If the signal level suddenly falls, the output of U1C follows, but the output of U1A remains high due to the slow decay of C23.

The output of U1D goes high as the U1C output falls below U1A, which will switch on Q6 or Q7 (depending on the state of open collector comparators U3A and U3B). The outputs of U3A and U3B go negative as the input voltage or board pin 38 exceeds the reference voltages for each comparator as determined by R36, R35, and R34. For an input above 7.7 VDC, both comparator outputs are negative, both Q6 and Q7 are prohibited from turn on by U1D, and the decay time is slow. Between +7.7 volts and +3 volts, U3A output is high which allows Q6 to be enabled by U1D output and the decay through the 68k R39 is medium (about 400 milliseconds). An input below +3 VDC causes both comparator outputs to go high allowing both Q6 and Q7 to be enabled. The decay is fast through R39 and R38 in parallel. An external ground on pin 41 will dump the AGC voltage, putting the receiver in a high gain status. The AGC signal may be over-ridden by a 0 to 6 VDC voltage on pin 34.

U1B provides an additional gain of 2 (by R43/R44) to output the receiver AGC voltage at pin 11.

This voltage controls the IF Filter board gain, maintaining a constant IF input level to the Audio Squelch board and consequently, a constant audio output level. The "S" meter output at pin 42 is adjustable by R44 to produce 4.7 volts into 10k ohms to ground when the AGC voltage is +6 volts. A delayed AGC signal to control Mixer board gain is produced by a current amplifier (U4D and Q9). The AGC voltage input is attenuated by R47/R48. The offset voltage which determines the voltage at which DAGC becomes active is set by R52; DAGC current gain is adjusted by R53.

5.1.1.6 Miscellaneous Circuits

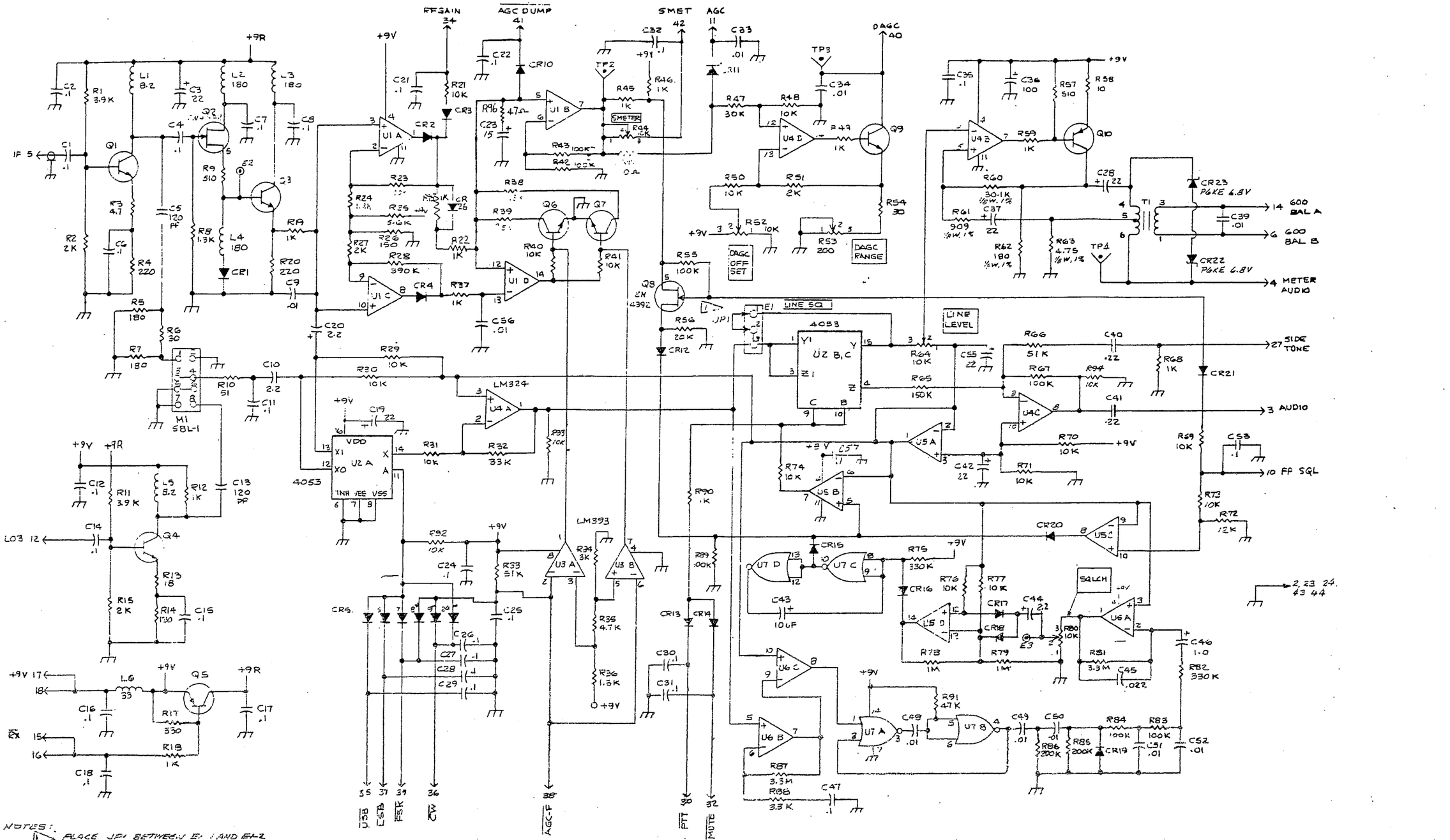
Diodes CR5, CR6, CR7, and CR24 control the U2A audio switch to direct product detector signals to the audio output circuits with a ground on pins 35, 36, 37 or 39 ($\overline{\text{USB}}$, $\overline{\text{CW}}$, $\overline{\text{LSB}}$, or $\overline{\text{FSK}}$). If no grounds are applied, the switch passes AM audio signals from the envelope detector. Diodes CR8 and CR9 from $\overline{\text{FSK}}$ and $\overline{\text{CW}}$ ground signal inputs cause U3A and U3B outputs to go high, resulting in a fast AGC decay rate. Q5 applies +9 volts to the 3rd LO amplifier, Q3, and to IF amplifier and envelope detector circuits (Q1, Q2, Q3), only in receive with a ground on pins 15 and 16.

AUDIO SQUELCH BOARD (601077-536-004)

SYMBOL	DESCRIPTION	PART NUMBER
C1,2,4,6-8,11,12, 14-18,21,22,24-32,35,47,53, 58	Cap., 0.1 µf, 63V	600302-314-013
C9,33,34,48-52, 56,57	Cap., 0.01 µf, 63V	600302-314-007
C40,41	Cap., 0.22 µf, 63V	600302-314-015
C5,13	Cap., 120 pf	600293-314-121
C3,19,37,38,42, 55	Cap., 22 µf, 25V	600297-314-016
C39	Cap., 0.01 µf	600189-314-018
C10,20,44	Cap., 2.2 µf	600297-314-006
C36	Cap., 100 µf	600297-314-032
C45	Cap., 0.022 µf	600268-314-012
C46	Cap., 1.0 µf	600202-314-007
C43	Cap., 10 µf	600202-314-018
C23	Cap., 15 µf	600202-314-020
CR1-21,24, 25	Diode, 1N4148	600109-410-001
CR22,23	Diode Pkge, 6.8V	600028-411-001
E1	Header, 3 Pin	600198-608-005
(E2,3)	Terminal, Small	600261-230-001
JP1	Jumper	600190-608-001
L1,5	Choke, 8.2 µH	600125-376-034
L2,3,4	Choke, 180 µH	600125-376-022
L6	Choke, 33 µH	600125-376-011
M1	Mixer, SBL-1	600008-455-001
Q1,3,4,6,7,9	Trans., 2N3904	600229-413-003
Q5,10	Trans., 2N3906	600116-413-002
Q2,8	Trans., 2N4392	600396-413-001
(Q8)	Trans. Pad, TO-18	600025-419-001
R13	Res., 18Ω, 1/4W, 5%	618094-341-075
R1,11	Res., 3.9k, 1/4W, 5%	639014-341-075
R2,15,27,51	Res., 2k, 1/4W, 5%	620014-341-075
R3	Res., 4.7Ω, 1/4W, 5%	647084-341-075
R4,20	Res., 220Ω, 1/4W, 5%	622004-341-075
R8,36	Res., 1.3k, 1/4W, 5%	613014-341-075
R9,57	Res., 510Ω, 1/4W, 5%	651004-341-075

AUDIO SQUELCH BOARD (601077-536-004)

SYMBOL	DESCRIPTION	PART NUMBER
R12,18,19,22,37,45, 46,59,68,90,49,95	Res., 1k, 1/4W, 5%	610014-341-075
R85,86	Res., 200k, 1/4W, 5%	620034-341-075
R25	Res., 5.6k, 1/4W, 5%	656014-341-075
R28	Res., 390k, 1/4W, 5%	639034-341-075
R29-31,40,41,48, 50,69-71,73,74,76, 77,92,93,94, 97, 98	Res., 10k, 1/4W, 5%	610024-341-075
R96	Res., 47Ω, 1/4W, 5%	647094-341-075
R91	Res., 47k, 1/4W, 5%	647024-341-075
R23,42,43,55,67, 83,84,89	Res., 100k, 1/4W, 5%	610034-341-075
R6,54	Res., 30Ω, 1/4W, 5%	630094-341-075
R58	Res., 10Ω, 1/4W, 5%	610094-341-075
R33,66	Res., 51k, 1/4W, 5%	651024-341-075
R56	Res., 20k, 1/4W, 5%	620024-341-075
R34	Res., 3k, 1/4W, 5%	630014-341-075
R35	Res., 4.7k, 1/4W, 5%	647014-341-075
R10	Res., 51Ω, 1/4W, 5%	651094-341-075
R14	Res., 130Ω, 1/4W, 5%	613004-341-075
R17	Res., 330Ω, 1/4W, 5%	633004-341-075
R32	Res., 33k, 1/4W, 5%	633024-341-075
R75,82	Res., 330k, 1/4W, 5%	633034-341-075
R88	Res., 3.3k, 1/4W, 5%	633014-341-075
R81,87	Res., 3.3 Meg, 1/4W, 5%	633044-341-075
R78,79	Res., 1.0 Meg, 1/4W, 5%	610044-341-075
R72	Res., 12k, 1/4W, 5%	612024-341-075
R5,7,62	Res., 180Ω, 1/4W, 5%	618004-341-075
R47	Res., 30k, 1/4W, 5%	630024-341-075
R65	Res., 150k, 1/4W, 5%	615034-341-075
R61	Res., 909Ω, 1/8W, 1%	690901-342-059
R60	Res., 30.1k, 1/8W, 1%	630121-342-059
R63	Res., 4.75Ω, 1/8W, 1%	647581-342-059
R26	Res., 150Ω, 1/4W, 5%	615004-341-075
R44,52,64,80	Pot., 10k	600063-360-010
R53	Pot., 200Ω	600063-360-005
R24,38	Res., 1.8k, 1/4W, 5%	618014-341-075
R39	Res., 7.5k, 1/4W, 5%	675014-341-075
R97	Res., 0Ω	600000-341-075
T1	Transformer, 600Ω	635234-501-001
TP2	Test Point, Red	600114-611-002
TP3	Test Point, Orange	600114-611-003
TP4	Test Point, Yellow	600114-611-004



Audio Squelch Board Schematic